Design of a high data-rate wireless communication on FPGA - Part one

G. Martin,[1]

[1]Haute École de la Province de Liège (HEPL), electronic and embedded systems, Liège, Belgium

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Abstract

This paper discusses about a high data-rate wireless communication implemented using a FPGA. The technologies chosen are QAM and OFDM. A first version with low data-rate has been developed on a *Zybo Z7* FPGA board using a digital carrier architecture. Future versions of the project will use more performant equipment and other architectures to increase both the carrier frequency and the data rate.

1 Introduction

Nowadays, the amount of data generated and consumed by digital devices increases constantly. Wireless communications must be more and more efficient and data-rate is a critical aspect. In this paper, we will compare several digital modulation techniques and choose the one that matches the most our application : a $1Gb/s$ wireless communication implemented using Field Programmable Gate Arrays (FPGA). As reference, *Bluetooth* has a data-rate of about $1Mb/s$ and Wi-Fi 802.11a reaches $54Mb/s$.[1] Frequency-division multiplexing will also be discussed.

This project will use FPGA technology because of its capability to compute processes quickly and the fact that it can deal with several processes in parallel.

2 Technology selection

2.1 Modulation techniques

Digital modulation techniques transfer data by changing the carrier signal properties : frequency, amplitude and phase. The associated techniques are called respectively Frequency-Shift Keying (FSK), Amplitude-Shift Keying (ASK) and Phase-Shift Keying (PSK) [2]. A more complex one called Quadrature Amplitude Modulation (QAM) applies variation to both amplitude and phase. It allows very high-order modulation schemes. Modulation order being the amount of different carrier states used.

2.1.1 Spectral efficiency

The spectral efficiency of a given digital modulation scheme gives the data-rate achieved by one Hertz of the modulated signal's bandwidth. This is a critical aspect for most of wireless communications systems.

Table 1 shows the spectral efficiency (in bits/s/Hz) of several modulation techniques. Quadrature Amplitude Modulation (QAM) allows high-order modulation with several hundreds of symbols and has a better spectral efficiency than PSK. Increasing the amount of symbols does not wider the bandwidth of the modulated signal, which means it increases spectral efficiency. The problem is that it will lead into a greater Bit Error Rate (BER) because the demodulator uses euclidean distance between the I-Q point measured and the theoretical constellation. Adding more symbols means less distance between the constellation's points which leads to greater chances to mistake a symbol for another.

Modulation	Efficiency (bits/s/Hz)
MSK	1
BPSK	1
QPSK	2
16-QAM	4
32-QAM	5
64-QAM	6
256-QAM	8

Table 1: Spectral efficiency of several modulation techniques [3]

2.1.2 Bit error rate

The BER measures the amount of errors in the communication and needs to be minimized. In digital modulation, the technique that offers the best BER is FSK, followed by QAM then PSK and the worst is ASK [3].

Furthermore, an error of one symbol using QAM-4 or QAM-256 means an error of respectively 2 bits and 8 bits. The more symbols in the constellation, the more bits fail. This is why it is more efficient to have an adaptive system that changes the modulation order according to the BER. The BER depends on both the modulation technique and the modulation order.

2.1.3 Modulation choice

The modulation that will be used for this project is the QAM because of its spectral efficiency. FSK has better BER characteristics but is way worse as far as spectral efficiency is concerned [3].

2.2 Frequency-division multiplexing techniques

In order to increase the data-rate, one can increase the amount of symbols in the modulation's constellation. The problem is that this approach has its limits because of the symbols discrimination. Another way is to spread the data flow on several channels, each one using a carrier at a different frequency. This technique is called Frequency Division Multiplexing (FDM). It also allows to share the spectrum between users and peripherals.

There are several FDM techniques but the most suitable one is called Orthogonal Frequency-Division Multiplexing (OFDM). This technology sends data through orthogonal channels, which are separated by the minimum frequency theoretically achievable. The spectrum value of one channel is zero at regular intervals and the OFDM uses this property by spacing two consecutive channels by the value of that interval. It means that the centre of a channel is placed precisely at a frequency where all other channels cancel [4]. This principle is illustrated by the figure 1.
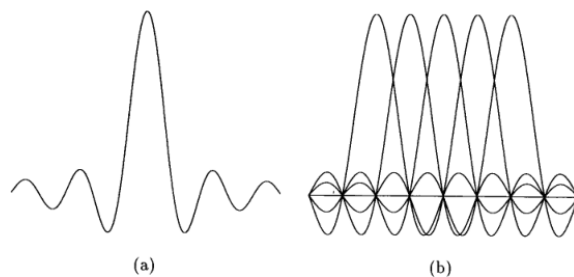

Figure 1: (a) An unfiltered QAM signal spectrum. (b) OFDM signal spectrum. [4]

This technique is the most efficient one but is also very difficult to implement. This is why we will be using an easier method to start the project. This method also uses several channels but the frequency interval between those is greater so they do not interfere with each others.

The fact of using several channels allows the communication to be faster because data is sent through various carriers. The bit-rate is directly proportional to the amount of channels used.

3 Simulations and developments

There are two carrier generation techniques : digital or analogical. The first one uses a Direct Digital Synthesiser (DDS) and all signals are digital until the end of the modulation. The second technique uses a carrier generated by a local oscillator. Mixers are used to apply the I and Q components from the constellation. The two techniques are showed on figure 2.
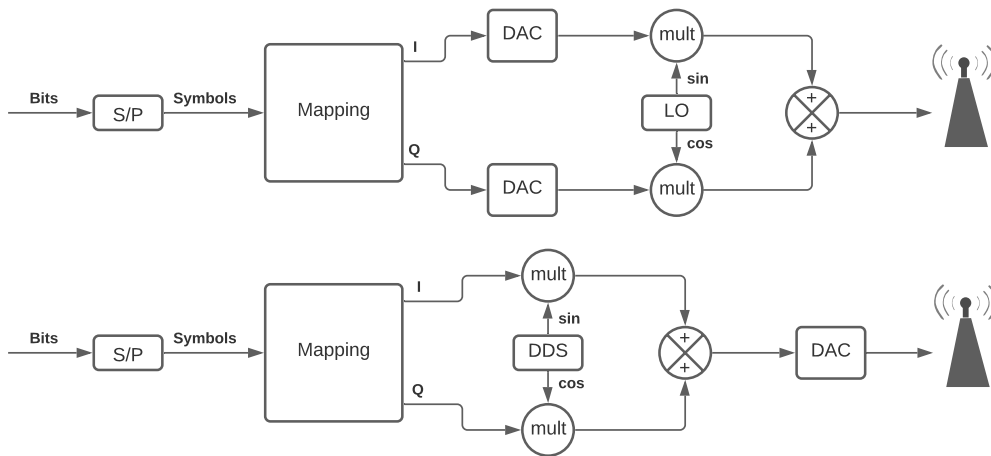

Figure 2: Analogical carrier (top) and digital carrier (bottom)[5]

3.1 Mapper

The mapper block in the figure 2 is composed of several Lookup Tables (LUTs) and is used to output I and Q values for a given symbol. It contains two LUTs (one for I and one for Q) for every modulation order.

The values in those lookup tables represent the constellation diagrams of every modulation scheme that will be used by the system. This means that all the carrier states (phase and amplitude of the modulated carrier because QAM is used) are defined inside the mapper.

3.2 Direct Digital Synthesiser

For the first technique development (bottom in figure 2), a DDS has been implemented in the FPGA using a sine wave LUT. The frequency of the output signal created can be configured using two methods : clock prescaling factor and the «frequency multiplier». The first reduces the clock frequency so each signal's sample is output for a longer time. The second jumps over several LUT values, by skipping samples, the signal frequency increases.

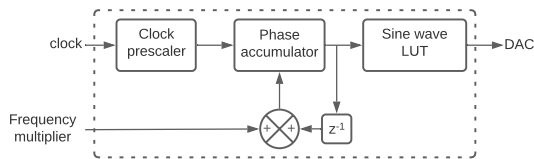Figure 3 shows the block diagram of the sine wave DDS.

Figure 3: Sine wave DDS block diagram

The sine wave values contained in the LUT have been computed using *Matlab*.

Using a Phase-Locked Loop (PLL) to feed the *clock* input could be a great improvement in order to generate a sine wave at a specific frequency. The limitations of the DDS block are still to be determined.

3.2.1 Theoretical generated frequency

The LUT used contains 256 samples which means that with a frequency multiplier and a prescaling factor of one, the generated signal will last for 256 periods of the clock signal. The equation 1 can be obtained using the same logic (with f_{out} the frequency of the generated sine wave).

$$f_{out} = \frac{f_{clock} \cdot freq\_mult}{256 \cdot prescaler} \quad (1)$$

3.2.2 Sine wave generated

The figure 4 shows the oscilloscope result of an approximatively $1MHz$ sine wave generated using the DDS technique explained above.
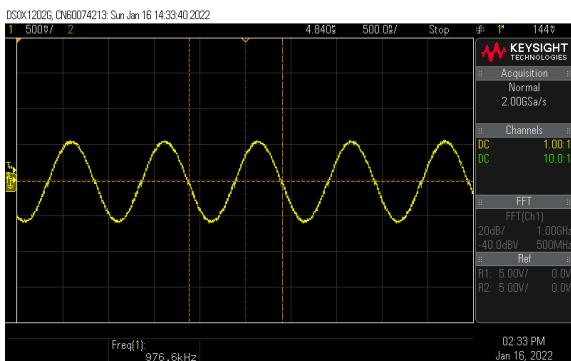

Figure 4: DDS generated sine wave

The measured frequency is $976.6kHz$ and the theoretical frequency obtained with equation 1 is $f_{out} = \frac{125\ 000\ 000 \cdot 4}{256 \cdot 2} = 976.5625kHz$ which means that at this range of frequency the sine wave generation is accurate.

3.3 Results on FPGA

A first version of QAM-4 with a $1MHz$ DDS generated carrier have been developed and tested on a *Zybo Z7* FPGA board. The symbol period is $100kHz$ which means the data-rate of this first test is $200kb/s$ (100.000 2-bits symbols per second).

The resources used are summarized in the table 2. It shows that this first version uses only a tiny portion of what is available on the chip. Another important thing to notice is that this project will later be using another FPGA with more resources (for example, it will have eight times more LUTs).

Resource	Amount used	% used
LUT	187	0.35%
FF	81	0.08%
BRAM	1	0.7%
IO	10	8%
PLL	0	0%
DSP	0	0%

Table 2: FPGA resources used

3.3.1 QAM-4 signals

The figure 5 shows the transition between two symbols on the modulated signal. The cursors are spaced by $256ns$ which is the quarter of the carrier's period (carrier frequency is $976.5625kHz$ as seen in subsection 3.2.2). Therefore, it corresponds to a 90 deg phase. As the two carrier states cross the x-axis on both the cursors, it means that the signal is shifted in phase by 90 deg.

The modulation scheme used for this example is QAM-4 so the amplitude between all the carrier states does not change.
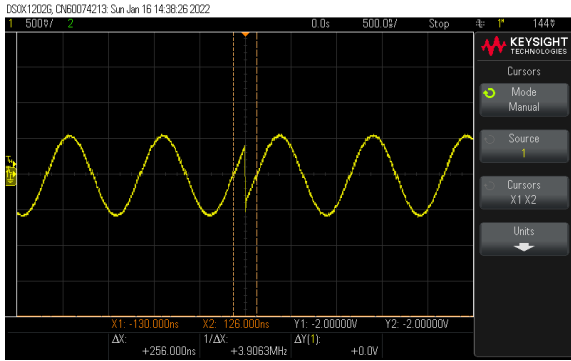

Figure 5: Transition between two carrier states

3.3.2 Data-rate measurement

The figure 6 shows the symbol period between the two cursors. Each symbol has a duration of $10.18\mu s$ which means the modulated signal contains approximatively one hundred thousand of symbols per second. As the modulation used in this test is QAM-4, each symbol contains two bits of data, which leads to a $200kb/s$ data-rate.
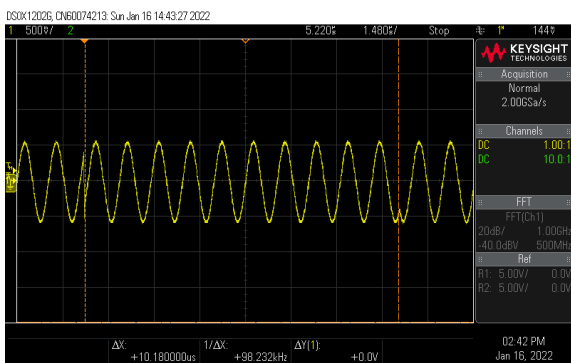

Figure 6: Symbol period of modulated signal

3.4 Spectrum simulation

As the carrier is still at a low frequency compared to what it should be in the future versions of the project, the modulated signal's spectrum has not been measured yet on the output of the FPGA.

A simulation using *Simulink* and *Matlab* has been made using the same system architecture as the one developed on the *Zybo Z7* board but with a $2.4GHz$ carrier and a symbol frequency of $1MHz$. The spectrum obtained is showed on the figure 7. It has a maximum value at the carrier frequency and several local minima separated by the symbol frequency.
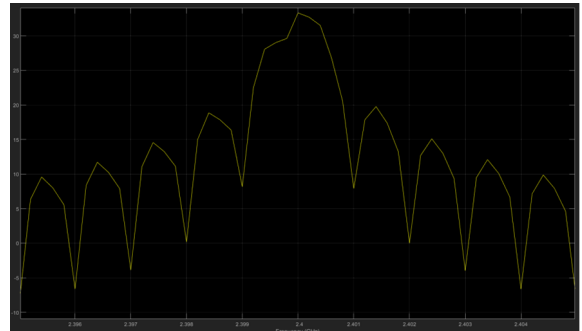

Figure 7: Simulated spectrum of the modulated signal

4 Conclusions

This paper described a work in progress. The major achievements here are the determination of the techniques that will be used in the future versions of the project and the discovering of the digital signal processing world using FPGA.

The future improvements to do are : increase the carrier frequency, pulse shaping implementation, adaptive modulation order as well as everything concerning the demodulator.

Implementing the mixed architecture from figure 2 may be useful in order to compare with the already developed solution. Its analog components may simplify a lot the VHDL code for the FPGA. The problem is that the mixers for I and Q must have the exact same characteristics or the modulation will not be a success.

References

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