FIRST USE IN A CUBESAT OF THE INNOVATIVE, FULLY QUALIFIED, RAD-HARD DIGITAL PROGRAMMABLE CONTROLLER (DPC)

Sebastien De Dijcker[2], Valéry Broun[2], Xavier Werner[3], Alain Van Esbeen[4], Thierry Van Humbeeck[4], Marc Bekemans[4], Marc Fossion[4], Jacques G. Verly[1]

[(1)] University of Liège, Dept. of Electrical Engineering and Computer Science, Liège, Belgium
[(2)] Haute Ecole de la Province de Liège, Engineering Department, Liège, Belgium
[(3)] University of Liège, Dept. of Aerospace and Mechanics, Liège, Belgium
[(4)] Thales Alenia Space, Charleroi, Belgium

1 INTRODUCTION

After the successful 26 April 2016 launch of the University of Liège OUFTI-1 educational 1-U CubeSat featuring, as primary mission, an amateur-radio D-STAR communication repeater, and some operation difficulties in orbit, the university started, on 6 July 2016, a new project aimed at building an OUFTI-2 taking advantage of the lessons learned.

Besides improving on OUFTI-1, the design of OUFTI-2 had to take into account a possible launch from the ISS, implying a change of battery configuration and significant related changes to the electrical power system (EPS). About one year into the project, one significant weakness remained, that of resistance to space radiation. The OUFTI-2 team examined several options that all preserved the use of MSP430 processors, especially in the on-board computer (OBC), such as considering different types of MSP430s and the addition of external memory with better resistance to radiation. However, on 4 Oct 2017, a discussion with Thales Alenia Space (TAS), Belgium, guided the team to a new, ideal solution. Indeed, upon the mutual realization that OUFTI-2 used MSP430s and that TAS's newly developed, radiation-hardened Digital Programmable Controller (DPC) was architected around the openMSP430, it became obvious that using the rad-hard DPC as the heart of the OUFTI-2 OBC would significantly increase the CubeSat reliability.

The paper successively describes the hardware architectures of OUFTI-2 and the DPC, the strategies of development of the OBC hardware and software, and the current state of development of OUFTI-2, ending with a brief conclusion.

2 HARDWARE ARCHITECTURE OF OUFTI-2

Figure 1 shows the block-diagram describing the hardware architecture of OUFTI-2. The main elements are: (1) electrical power system (EPS) with associated solar panels and batteries; (2) on-board computer (OBC), based on the DPC; (3) communication system (COMM), providing D-STAR voice & data user communication (the main payload), AX.25 telecommand & telemetry (TC/TM), and beacon (BCN) Morse-code transmission, as well as VHF & UHF radiofrequency (RF) electronics; (4) secondary payloads for attitude measurements (IMU) and for radiation measurements (RAD).

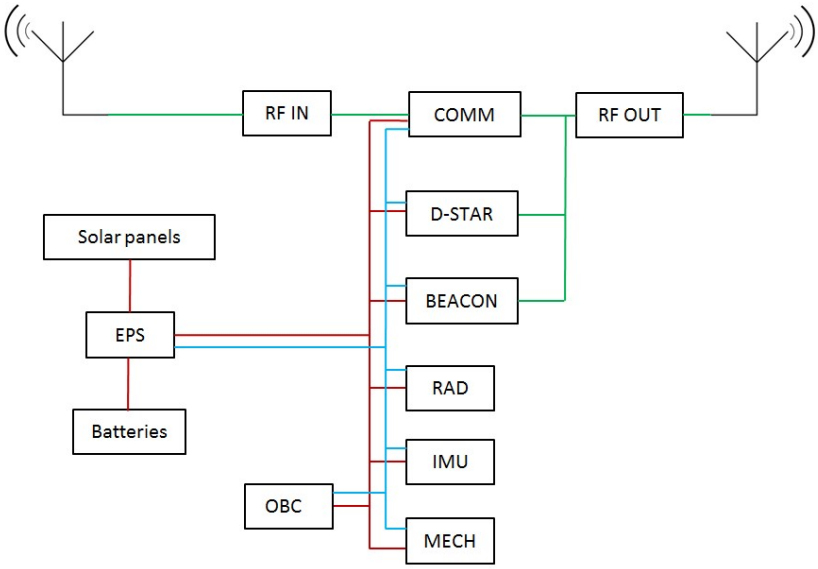

Figure 1. Block-diagram of hardware architecture of OUFTI-2.

Figure 2 shows an exploded CAD view of the 1U CubeSat OUFTI-2. The structure – from ClydeSpace - contains 5 electronic boards (EBs), i.e. printed circuit board (PCBs) populated with various components. From bottom to top, one finds the electronic boards corresponding to the following: (1) RAD board, with the RAD secondary payload, (2) OBC board, with the DPC and its peripheral components, (3) EPS board, with a box containing the pair of batteries, (4) BCN + IMU board, with the BCN part of the COMM, and the IMU secondary payload, (5) COM board, with the primary payload D-STAR and the AX-25 system for TC/TM. Figure 2 also shows other elements: antennas, passive attitude determination and control system (ADCS) (consisting of a permanent magnet and hysteretic rods), antenna deployment mechanism (MECH), and solar panels.

Besides using the DPC for its OBC, OUFTI-2 features several modifications/improvements over its predecessor. The structure and solar panels are now from ClydeSpace. Within the communication system (providing D-STAR voice & data user communication, AX.25 TC/TM, and beacon (BCN) Morse-code transmission), the BCN is fully redesigned, providing higher power efficiency, and the D-STAR system now provides a beacon mode. The EPS now uses a bus that is semi-regulated rather than unregulated. The DPC added new constraints to the design of the EPS. The removal of some redundant elements (such as the second OBC and its dedicated electronic board) also freed up some space, allowing new secondary payloads, including one designed to test the effect of various shields against ionizing radiation. The electronics for this last payload has three separate, identical areas, respectively without shield, with a classical shield, and with a multilayer shield. In each area, the electronics measures the time progression of the threshold of a RADFET. The value of the threshold and the temperature give an estimate of the total dose received.

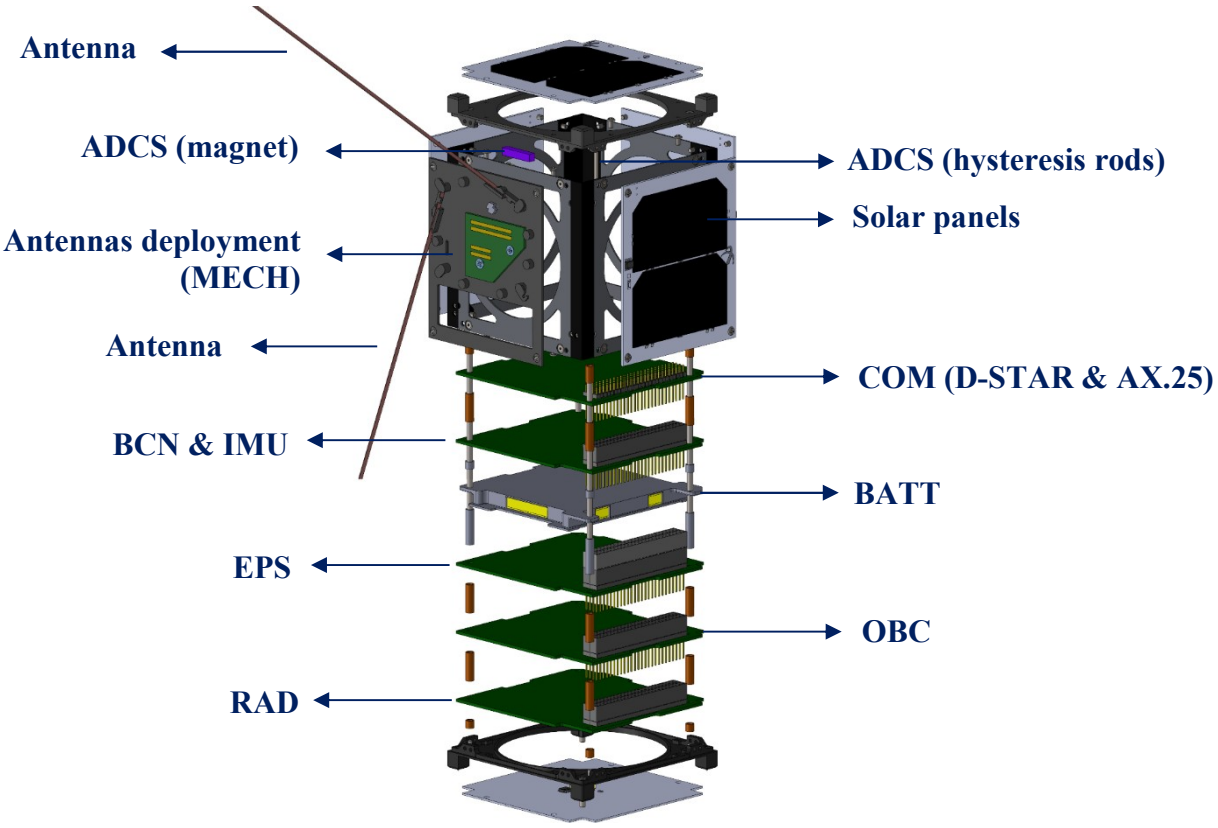

Figure 2. CAD model of OUFTI-2.

3 HARDWARE ARCHITECTURE OF DPC

The Digital Programmable Controller (DPC) is a mixed-mode system-on-chip developed by Thales Alenia Space (TAS). It integrates a large set of functions for managing sensors, actuators, power systems, communication systems, etc. It is built around 3 distinct cores, the so-called SSM, COM, and RAS controllers, all located on the same die, but with each having its own (openMSP430-based) CPU. While these 3 controllers can communicate, they are maximally decoupled to increase the "determinism" of the task(s) that each runs. The DPC can be used without a real-time operating system, as sufficient processing resources are available to run several tasks fully in parallel. The DPC integrates a large variety of peripherals and hardware accelerators such as ADC, DAC, PWM generators, timers, SPI, I^2C, UART, MIL-STD-1553 bus, CAN-bus, hardware 32 bits MACC, and hardware 32 bits divider & barrel shifter. Importantly, especially for OUFTI-2, the DPC is rad-hard, with experimentally-observed absence of drift up to at least 60 kRad. It was carefully designed to be usable in a wide variety of microcontroller space applications. Producing a single ASIC that is usable in a multitude of applications makes a lot of sense for space applications with low volumes, because a single component can be qualified once-and-for all, especially in terms of rad-hardness. Since February 2017, the DPC is qualified according to ESA standard (ESCC 9000).

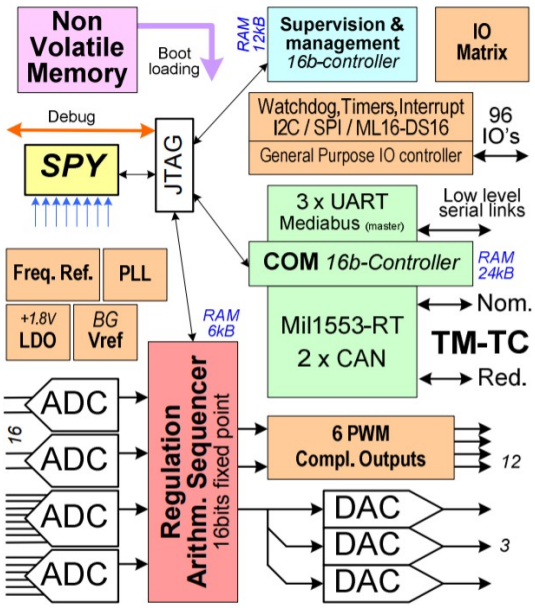

Figure 3. Architecture of TAS's Digital Programmable Controller (DPC).

The three-operational-cores concept must definitely be distinguished from the "multi-cores" architectures found in common personal computer processor devices, where several instances of a single CPU sharing the same memories and peripherals are implemented next to each other in order to boost the processing capacity and performance. In the DPC circuit, special care has been taken to avoid fault propagation by keeping apart (i.e. segregating) the functions in terms of criticality, real-time requirements, and responsiveness. As such, each of them, implemented in one of the three operational cores, can proceed autonomously with normal or degraded operation, even in case of failure of an adjacent process running in a neighboring core.

The target is to obtain a high reliability level by relying on hardware segregation. In the DPC, each core might have its own activity time-range class, individually from the others. There is no need to have a central operating system managing, for all the CPUs, the tasks and the different beat events. Indeed, each core has its own program and data memories and has full and permanent access to its own peripherals. Hence predictability of execution time, quick interruption management, and tight synchronization to periodic events can easily be guaranteed.

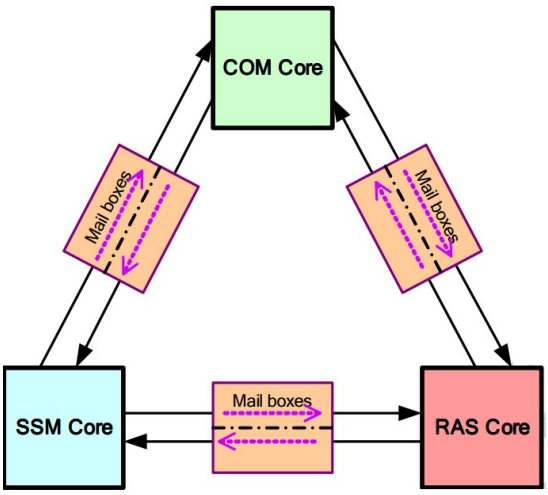

Figure 4. The three DPC cores (COM, SSM, and RAS) and the exchanges between them.

In order to exchange information between them, the cores can use the built-in mailbox function that is designed to allow data transfer in any direction and from any core to any core. Each exchange is accomplished without disturbance and under the control of both the sender and the receiver.

4 STRATEGY OF DEVELOPMENT OF OBC HARWARE

The on-board computer (OBC) of OUFTI-2 controls all of the satellite subsystems. Figure 5 shows the architecture of the OBC.

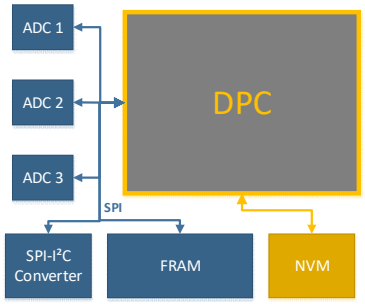

Figure 5. Architecture of on-board computer (OBC) of OUFTI-2.

The architecture comprised the following main elements:

- Programmable Digital Controller (DPC) described above;
- Non-volatile memory (NVM) for storing the DPC code;
- 3 analog-to-digital converters (ADCs) used to get various measurements from all sub-systems;
- Ferroelectric RAM (FRAM) for storing the measurements and the satellite log;
- SPI bus used as the main bus for the OBC;
- SPI-to-I^2C converter used for communication with the battery subsystem (BATT).

Besides the 3 ADCs on the OBC board, there are 3 other ADCs on other boards, namely those corresponding to the COM and EPS subsystems. Several different analog signals can be routed to each particular ADC via a multiplexer.

The SPI-to-I^2C converter was required as a result of the fact that the batteries that we selected (mainly as a result of a possible deployment from the ISS) use the I^2C protocol for communications.

The OBC communicates with the various electronic components and subsystems of the satellite via an SPI (Standard Peripheral Interface) bus. It is used for:

- reading the digital measurements provided by the ADCs;
- writing to, and reading from, the FRAM;
- communicating with the subsystems BCN, D-STAR, IMU, and RAD;
- communicating with the subsystem BATT via the SPI-to-I^2C converter.

On the DPC, the SPI is managed by the USI (Universal Serial Interface). The DPC's USI provides several types of synchronous communications (SPI, I^2C, etc.). This USI can be configured to use different timings, polarities, and other parameters of such communications.

Figure 6 shows the architecture of the communication links throughout the satellite, via SPI or I^2C, as appropriate. The figure essentially shows how the DPC USI is connected to the various electronic components and subsystems of the satellite.

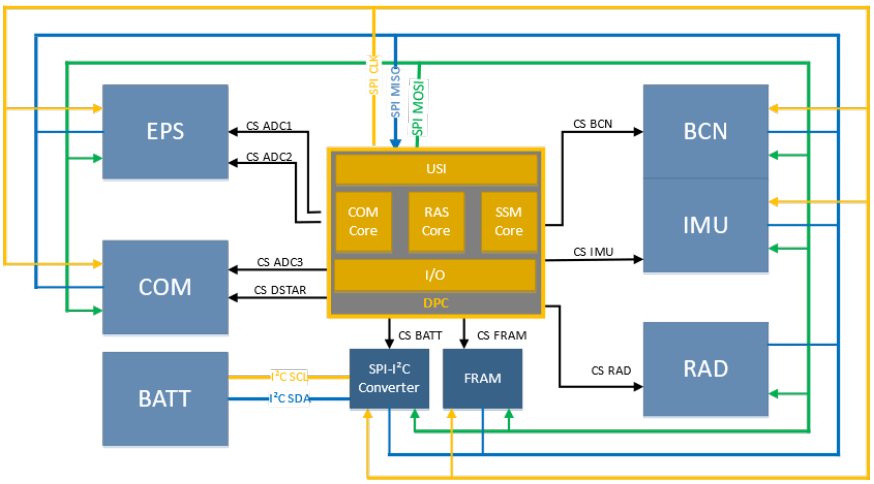

Figure 6. Architecture of communication links, either SPI or I^2C.

As illustrated in the figure, there are, in total, 9 SPI peripherals that are controlled by the SSM core of the USI:

- 3 ADC converters located on the COM and EPS boards;
- subsystems BCN, D-STAR, IMU, and RAD;
- subsystem BATT via SPI-to-I^2C converter;
- FRAM located on OBC board.

5 STRATEGY OF DEVELOPMENT OF OBC SOFTWARE

The OBC software is developed on a TAS DPC Reference Kit (DRK). Figure 7 shows the DRK, as seen from below, so as to show the DPC.

To move from the initial software development on the DRK to the actual OBC electronic board, we use the following strategy. We are developing a prototype OBC electronic board where the DPC is displaced to a small daughter card that can be plugged, in a mezzanine way, on the OBC board. This strategy allows us to avoid soldering and unsoldering the DPC if one needs to make changes to the rest of the OBC board.

While we use, for this prototyping, a DPC in a plastic package (Model CQFP256) and soldered on the small mezzanine board, we will use, for the flight model, a DPC in a BGA 16*16 plastic package and directly soldered, of course, to the OBC board.

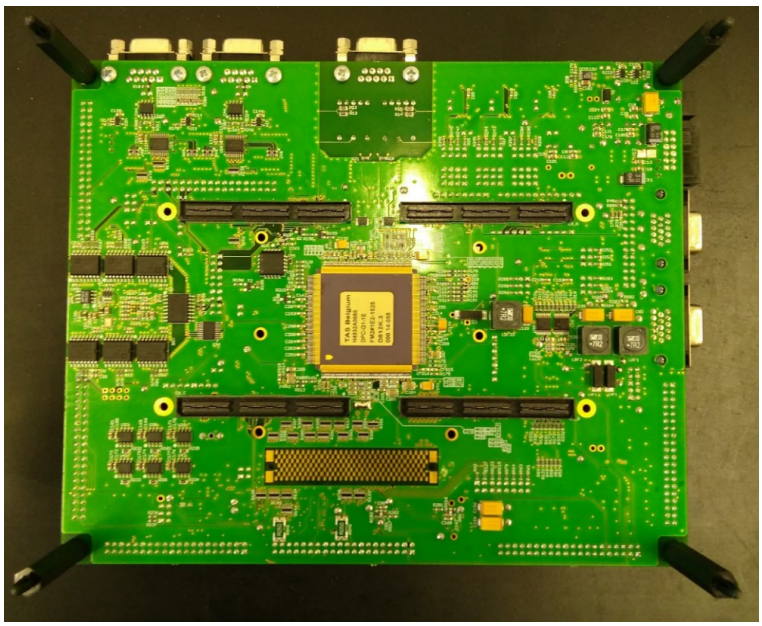

Figure 7. View of DRK from below, showing the DPC at the center.

Figure 8 shows a CAD view of one assembly/arrangement that we are using to develop and test the OBC code. The figure shows, from top to bottom, the daughter board with the CQFP256 DPC, the main OBC board (which the daughter board is plugged into), and the EPS board used for powering the two previous boards.

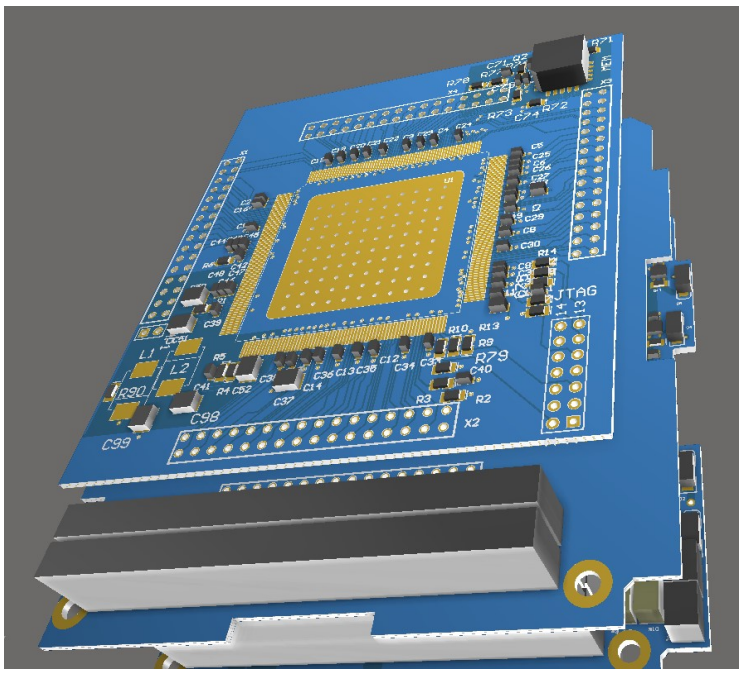

Figure 8. CAD view of assembly of daughter board with DPC, main OBC board, and EPS board (from top to bottom).

6 CURRENT STATE OF DEVELOPMENT OF OUFTI-2

We have finalized the overall hardware architecture of the whole satellite, and the hardware architecture of each of the subsystems. We have built prototypes of most of these subsystems. Some have been tested and others are currently (as of spring 2018) under test. We have, in house, the structure, solar panels, and ISS-compatible batteries.

We have finalized the software architecture of the satellite. We have developed a detailed implementation plan, and the various software modules are currently (as of spring 2018) being coded and tested systematically.

7 CONCLUSIONS

As of spring 2018, we have finalized the hardware and software architectures of the 1U CubeSat OUFTI-2 (having an amateur-radio D-STAR telecommunication repeater as its main payload), and their implementations and tests are at a fairly advanced state.

The use of DPC from Thales Alenia Space (TAS), Belgium, will provide exceptional hardware resistance to space radiation for a 1U CubeSat. The switch from a redundant dual processor architecture to the DPC required a significant initial feasibility study to make sure that OUFTI-2 could use it. In particular, we had to make sure that the 1U CubeSat would provide enough electrical power to operate the DPC. The use of the DPC also required several changes in the hardware and software architecture.

With all the software changes that we wanted to implement based upon the lessons learned from OUFTI-1, and with the switch to the DPC, we decided to rewrite the OBC software essentially from scratch. Of course, some software modules can be re-used such as those related to D-STAR communications. Of course, the fact that the predecessor OUFTI-1 and the DPC are both based on the MSP430 made the transition to the DPC much easier.

8 REFERENCES

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