GaN-on-Porous Silicon for RF applications

Gilles Scheen[#λ1], Romain Tuyaerts[#*], Pieter Cardinael[*], Enriqué Ekoga[#], Khaled Aouadi[#], Christophe Pavageau[#], Amin Rassekh[#], Massinissa Nabet[*], Sachin Yadav[§], Jean-Pierre Raskin[*], Bertrand Parvais[§§], Mostafa Emam[#]
[#]Incize, Louvain-la-Neuve, Belgium,
[λ]Service Electronique, HEPL, Liège, Belgium
[*]ICTEAM, UCLouvain, Louvain-la-Neuve, Belgium
[§]imec, Leuven, Belgium,
[$]ETRO, Vrije Universiteit Brussel (VUB), Brussels, Belgium,

[1]gilles.scheen@incize.com

***Abstract* — Gallium nitride (GaN) is a promising semiconductor for RF and high-power applications. However, its large-scale industrialization is hindered by several challenges, primarily the lack of cost-effective, high-performance handle substrates. Sapphire and SiC present high performances, but their use in electronic applications is limited due to their high cost. GaN-on-Si substrates are more affordable but suffer from high substrate-induced RF losses. We introduce an innovative method to mitigate the substrate losses. Porous silicon is known for decades for its high RF performance but its integration is challenging. We performed porosification of the handle silicon substrate after the fabrication of the RF devices, from the backside, preserving the high quality of the GaN layers and the low cost of GaN-on-Si, while boosting the RF performances. We achieved harmonics H2 =-140 dBm at Pout=15 dBm, RF losses under 0.1 dB/mm at 5 GHz, and an effective resistivity higher than 8 kΩ·cm at 5 GHz.**

***Keywords* — Effective dielectric permittivity, effective resistivity, harmonic distortion (HD), RF and microwave losses, porous silicon (PSi), GaN-on-Silicon (GaN-on-Si) technology, trap-rich (TR), RF characterization, RF substrate.**

I. Introduction

Gallium Nitride (GaN) has emerged as a promising semiconductor material for high-frequency and high-power applications due to its unique material properties. One of the challenges in GaN technology is to reduce the manufacturing cost while maintaining high device performance. GaN-on-Si technology is a potential solution to fulfil that challenge, as it allows GaN devices to be fabricated on inexpensive and large-area silicon substrates compared with sapphire or SiC wafers. This technology offers furthermore the ability to leverage existing silicon processing infrastructure.

Recent advances in GaN-on-Si technology have led to significant improvements in device performance and high electron mobility transistors (HEMTs) fabricated using GaN-on-Si technology have demonstrated competitive RF performance compared to HEMTs fabricated on other substrates [1].

One of the challenges in GaN-on-Si technology is the epitaxial growth of an AlN layer on the Si handle substrate. The AlN layer is typically used as a nucleation layer to reduce the lattice mismatch between GaN and Si and enable subsequent growth of high-quality III-N layers. However, the high-temperature AlN and subsequent III-N epitaxial process can result in diffusion of Al and Ga atoms into the Si handle substrate. This in turn leads to formation of a parasitic surface conductive (PSC) layer near the Si/AlN interface resulting in the degradation of the substrate RF performance. Reference [2] presented a detailed study of substrate losses and non-linearities for GaN-on-Si HEMTs which takes both the epitaxial and fabrication process steps into account. Chang et al. [3] demonstrated that these losses were dominated by the presence of a parasitic surface conductive (PSC) layer at the AlN/Si interface. Several approaches have been proposed to mitigate contamination of the Si handle substrate during the growth of the AlN layer. For example, the use of a thin SiN layer between the Si substrate and the AlN layer can prevent inter-diffusion at the interface [4].

Reference [3] further showed that the growth temperature of the AlN during a metal organic chemical vapor deposition (MOCVD) process impacts RF loss in the AlN/Si template. The authors observed that a low growth temperature of the AlN nucleation layer can reduce the RF losses in the AlN/Si template but can result in low crystalline quality. Therefore, optimizing the growth temperature of the AlN nucleation layer is crucial to obtain a balance between crystalline quality, morphological quality, and RF loss for the epitaxial growth of the complete GaN-on-Si RF device structure.

The PSC layer phenomenon also appears in RF-SOI technology and significantly degrades the RF performance of electronic circuits, although the origin of this layer is not the same as in GaN HEMTs. To minimize the impact of the PSC layer, a trap-rich layer (usually composed of polysilicon) is introduced at the SiO_2/Si interface during substrate fabrication to trap charge carriers and thus avoiding the formation of a PSC layer [5].

Introducing a trap-rich polysilicon layer is incompatible with GaN-on-Si technology as the epitaxy of the GaN HEMT stack requires a monocrystalline (111) silicon substrate for the epitaxy.

As an alternative to the TR layer, porous silicon (PSi) has been proposed for several decades in RF-SOI technologies [6]. Silicon porosification is performed by partial electrochemical dissolution (anodization) of bulk silicon. PSi achieves high effective resistivity, low permittivity, low losses, low crosstalk

levels, and high linearity. With all these properties, PSi is a promising candidate for RF handle substrates.

Recently, we presented an innovative technique to integrate high-quality porous silicon (PSi) after the fabrication of RF circuit (POST-PSi) on SOI wafers [7], before the packaging steps. The principle, described in Fig. 1, is to take a fully processed substrate, and perform the silicon porosification from the backside. Operating at the end of the value chain ensures transparency for upstream players, thereby minimizing the challenge of industrializing this new approach. In POST-PSi technique, the frontside is not involved in the porous layer formation. Therefore, the integrity of the RF circuitry is not compromised by the porosification process.

In this work, the POST-PSi technique is applied to an epitaxial AlN-on-Si substrate to transform it into AlN-on-Porous Silicon (AlN-on-PSi). This substrate was used as reference in this work because most of the RF losses originate from AlN growth in GaN-on-Si technology [3]. The comparisons are made in terms of : 1) the effective substrate electrical parameters extracted through the direct S-parameter measurements of coplanar waveguides (CPW) over a wide frequency range from 10 MHz to 5 GHz; 2) the substrate linearity performance at a fundamental frequency of 0.9 GHz, in terms of the harmonic distortion (HD) generated by the field-dependent substrate below the CPW line and 3) the thermal stability of RF performances over a temperature range from 25°C to 225°C.

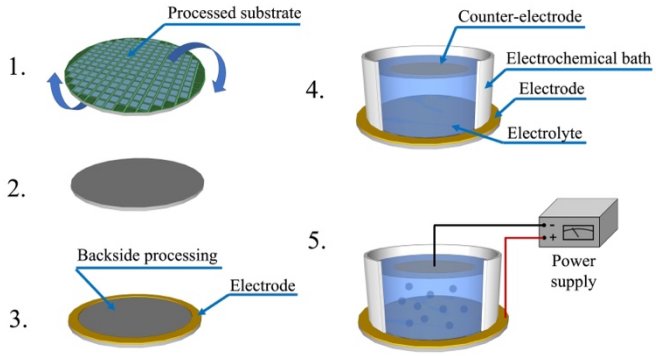

Fig. 1. Schematic of POST-PSi fabrication process: 1. The starting substrate is a fully processed substrate. 2. The frontside is glued on a carrier and not involved in the POST-PSi fabrication process. 3. A mask and an electrode are used on the backside for a porosification localized under the areas of interest. 4. Schematic of an adapted electrochemical cell. 5. Postprocess electrochemical porosification.

II. Experimental

A. *Reference substrate*

The AlN-on-PSi substrate is compared with an AlN-on-(HR-Si) reference substrate, typically used for RF applications. This reference AlN layer is grown on highly resistive (3-6 kΩ·cm) 200 mm-diameter Czochralski (CZ) Si (111) wafers by MOCVD. A 1-µm-thick layer of aluminum is deposited on the frontside by physical vapor deposition (PVD) and patterned by photolithography for the definition of the CPW lines.

B. *AlN-on-PSi Substrate fabrication*

An AlN layer grown on highly conductive (10-20 mΩ·cm) 200 mm Czochralski (CZ) Si wafers is used as a starting substrate. While high-resistivity Si is typically used in GaN-on-Si for RF applications to mitigate substrate losses, conductive silicon substrates are needed for the porosification by electro-chemical etching, and can be preferred for processing given their lower brittleness. A 1.5-µm-thick layer of aluminum is deposited on the frontside by physical vapor deposition (PVD) and patterned by photolithography for the definition of the CPW lines. The sample is then temporarily bonded to a quartz carrier wafer to allow a backside grinding, and to ensure protection of the devices on the frontside. A 2 µm-thick aluminium layer is deposited by e-beam evaporation on the backside and patterned in inter-die regions to improve homogeneity of the porosification on large samples. A polymer mask is then deposited and patterned to protect the aluminum layer, and to localise the porosification of porous pockets under the areas of interest (Fig. 2).

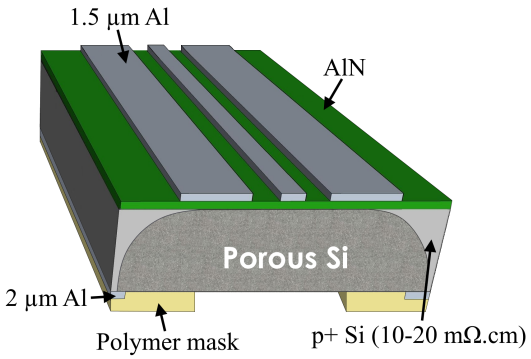

Fig. 2. Schematic of a CPW transmission line fabricated on AlN-on-POST-PSi substrates.

The porosification from the backside is performed in an adapted electrochemistry cell. Its particularity lies in making electrical contact with the silicon substrate at the edges of its backside, not involving the frontside and therefore not affecting the RF circuits. PSi is prepared by anodization in a 75:25 volume solution of HF(49%):isopropanol. The formation of porous silicon is isotropic. The applied total current is adjusted to have a current density of 70 mA/cm² at the interface between PSi and bulk Si. The anodization is performed until the pores reach the AlN layer used as an etch-stop layer. The porosification can then be pursued to enlarge the porous pocket if desired. After debonding, the sample is annealed at 150°C for 2 hours under an oxygen-rich atmosphere to oxidize and stabilize the porous Si.

C. *RF characterization*

We performed small signal (S-parameters) and large signal (harmonic distortion) on-wafer measurement on CPW lines having a width of 26 µm, a gap of 12 µm, for a total length of 2.15 mm. On-wafer measurements of CPW lines were performed using a Keysight 2-port performance network analyzer (PNA)-X vector network analyzer and a pair of ground-signal-ground (GSG) |Z| probes from FormFactor.

From the measured S-parameters, we extract RF losses, the effective resistivity (ρ_{eff}), and substrate relative permittivity ($\varepsilon_{r,sub}$) up to 5 GHz, using the method described in [8]. The same CPWs are also measured under large RF signal conditions to evaluate the harmonics distortion induced by the nonlinear properties of the substrates. Large signal measurements of the CPW lines were performed on wafer based on the setup from [9] and using an Agilent 4-port PNA-X vector network analyzer. The HD setup achieved detection of harmonic levels for a fundamental signal frequency of 0.9 GHz as low as −160 dBm for a maximum input power of 42 dBm.

III. Results and Discussions

A. *Morphology characterization*

Fig. 3 shows a cross-sectional view of a locally etched porous silicon substrate at the AlN/handle substrate interface. The PSi material grows throughout the entire substrate thickness from the backside up to the AlN layer. However, a thin layer of 10-20 nm thickness remains unporosified. We attribute this to a lower conductivity of the substrate at the interface, preventing the passage of the electrical current required for the porosification process. The reasons for this decrease in conductivity require further investigation, which could stem from dopant diffusion from the silicon into the AlN layer during substrate fabrication. It is worth noting that the presence of this layer does not appear to have a negative impact on RF loss.

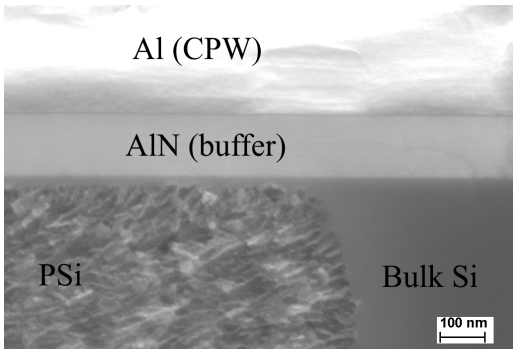

Fig. 3. Cross-sectional view of POST-PSi substrate magnified at the AlN/handle substrate interface, under a ground line of a CPW.

B. *Small-signal S-parameters*

Fig. 4 illustrates the comparison of the attenuation constant (α), the effective resistivity (ρ_{eff}), and the relative permittivity of the substrate ($\varepsilon_{r,sub}$) measured on the AlN-on-PSi and AlN-on-(HR-Si).

AlN-on-PSi substrate presents significantly higher effective resistivities and lower line losses than the AlN-on-Si substrate. The porosification of the handle substrate caused its resistivity to increase from 10-20 mΩ.cm to 10 kΩ.cm at 1 GHz. Such a high ρ_{eff} value can generally be considered to constitute a quasi-lossless substrate [10]. The reference AlN-on-HR-Si substrate shows a ρ_{eff} value of less than 1 kΩ.cm, although the initial resistivity of the HR-Si was 3-6 kΩ.cm. This drop in effective resistivity in HR-Si is attributed to the PSC layer [2,3]. The attenuation constant for the AlN-on-PSi substrates at 5 GHz are about 0.09 dB/mm compared with 0.3 dB/mm for HR Si handle substrate.

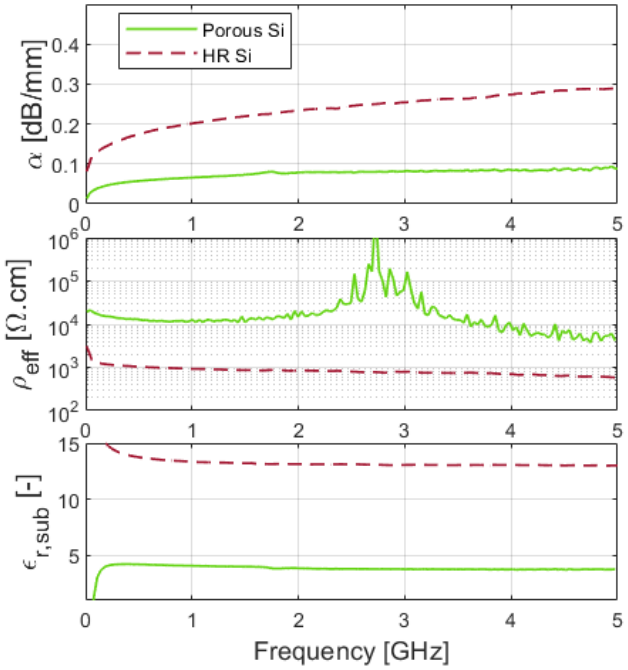

Fig. 4. Effective electrical substrate parameters extracted from wideband S-parameter measurements of RF CPW-lines at 25 °C for AlN-on-HR-Si and AlN-on-PSi Substrates. Top: CPW line losses per unit length. Middle: effective substrate resistivity. Bottom: substrate relative permittivity.

Porous silicon is a matrix composed of silicon and air. Thus, the permittivity of porous silicon is between the low permittivity of air ($\varepsilon_r \approx 1$) and the high permittivity of bulk silicon ($\varepsilon_r \approx 11.7$). Greater porosity results in a permittivity closer to that of air.

Our AlN-on-PSi samples present effective relative permittivity of approximately 3.75. The permittivity reduction offered by the PSi samples is desirable to reduce the parasitic substrate capacitance and coupling, especially at high frequencies where the substrate capacitance is the dominant coupling mechanism.

C. *Large-signal harmonic distortion*

Fig. 5 shows the 2nd and 3rd harmonic distortion components H2 and H3 of the CPW lines as a function of the output power at 0.9 GHz.

Very low levels of harmonics are observed on porous silicon (H2= -140 dBm and H3= -118 dBm at Pout= 15 dBm), which are significantly lower than what is observed on the HR-Si handle substrate (H2= -71 dBm and H3= -81 dBm at Pout= 15 dBm). Such low harmonic levels in porous handle substrates are comparable to those obtained on RF-SOI substrates porosified with the same method [7]. This improved linearity for PSi is explained by the tight pinning of the Fermi level throughout the entire volume of the PSi.

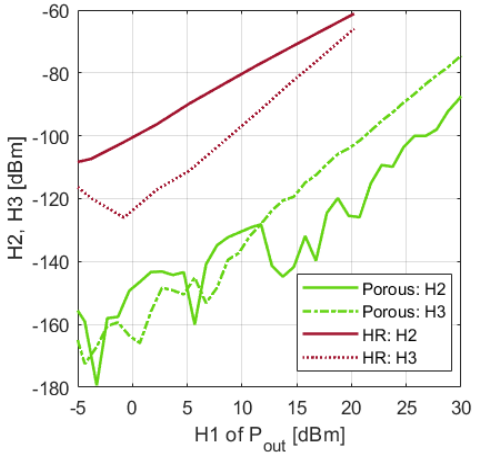

Fig. 5. Comparison of the measured HD levels induced along a 2.15 mm-long CPW line implemented on the two substrates under consideration. The fundamental frequency is 0.9 GHz and the lines are biased with 0 V DC.

D. Small- and large-signal electrical parameters at high temperature

RF losses at different frequencies, and H2 and H3 levels at H1=15 dBm, can be seen in Fig. 6 as a function of temperature, measured for a 2.15 mm long CPW line.

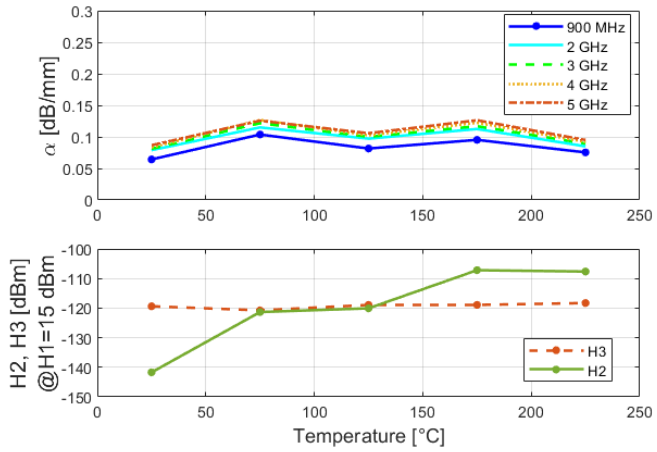

Fig. 6. Measured (top) CPW line losses per unit length and (bottom) CPW H2 and H3 levels at +15 dBm of H1 component on GaN-on-Porous Si versus substrate temperature from 25°C to 225°C at 0 V DC bias.

The attenuation constant α remains stable in the measured temperature range. However, since the metal loss in the CPW line also changes with temperature, the impact of the substrate is difficult to extract.

The porous silicon handle substrate becomes less linear as the temperature is increased, mainly due to the increase in H2 level. Indeed, the level of H3 remains stable with temperature. Although the H2 level in AlN-on-PSi substrate increases by 30 dBm between 25 °C and 225 °C, it remains very low, providing sufficient linearity performance for modern RF applications.

IV. Conclusion

In this work, the RF electrical performances of an innovative AlN-on-Porous silicon substrate were investigated and compared with the AlN-on-(HR-Si) substrate. In this innovative POST-PSi technique, local porosification of pockets of high-quality RF PSi-substrate are formed beneath the RF devices of interest. Only the substrate backside is involved in the porosification process which is strongly compatible with foundry-level processes. POST-PSi provides high RF electrical performances with low relative effective permittivity (~3.75), a high effective resistivity (above 8 kΩ.cm) and very low levels of harmonics (H2= -140 dBm and H3= -118 dBm at Pout= 15 dBm). AlN-on-PSi also provides very high linearity and stability with temperature from 25°C to 225°C. With the combination of low permittivity, high effective resistivity and high linearity, POST-PSi technology is an excellent candidate to enable high performance RF GaN-on-Si technology.

Acknowledgment

This research has been supported by the Win4Company funding of the Walloon Region (GaNGSTER project) and the Fonds pour la Formation à la Recherche dans l'Industrie et dans l'Agriculture (FRIA), FNRS, Belgium.

References

[1] H. W. Then, et al, "*3D heterogeneous integration of high performance high-K metal gate GaN NMOS and Si PMOS transistors on 300mm high-resistivity Si substrate for energy-efficient and compact power delivery, RF (5G and beyond) and SoC applications*," *2019 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2019, pp. 17.3.1-17.3.4

[2] S. Yadav, P. Cardinael, M. Zhao, K. Vondkar, A. Khaled, R. Rodriguez, B. Vermeersch, S. Makovejev, E. Ekoga, A. Pottrain, N. Waldron, J.-P. Raskin, B. Parvais and N. Collaert, "*Substrate RF Losses and Non-linearities in GaN-on-Si HEMT Technology*" *2020 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2020, pp. 8.2.1-8.2.4

[3] S. Chang, M. Zhao, V. Spampinato, A. Franquet, T. Do, A. Uedono, Luong, T. Wang and L. Chang (2020), "*The Influence of AlN Nucleation Layer on Radio Frequency Transmission Loss of AlN-on-Si Heterostructure*". Phys. Status Solidi A, 217: 1900755

[4] A. W. Hanson, J. C. Roberts, E. L. Piner, and P. Rajagopal,"*III-nitride material structures including silicon substrates,*" ed: Google Patents, (2007).

[5] D. Lederer, R. Lobet, J.-P. Raskin, "*Enhanced high resistivity SOI wafers for RF applications*" 2004 IEEE International SOI Conference (IEEE Cat. No. 04CH37573), 46-47

[6] M. Rack, Y. Belaroussi, K. Ben Ali, G. Scheen, B. Kazemi Esfeh and J. -P. Raskin, "*Small- and Large-Signal Performance Up To 175 °C of Low-Cost Porous Silicon Substrate for RF Applications,"* in *IEEE Transactions on Electron Devices*, vol. 65, no. 5, pp. 1887-1895

[7] G. Scheen, R. Tuyaerts, M. Rack, L. Nyssens, J. Rasson, M. Nabet, J.-P. Raskin, "*Post-process porous silicon for 5G applications, "* Solid-State Electronics, Volume 168, 2020, 107719

[8] D. Lederer and J.-P. Raskin, Solid-State Electron., vol. 49, no. 3, pp. 491–496, 2005.

[9] D. C. Kerr, J. M. Gering, T. McKay, M.S., C. Roda Neve, and J.-P. Raskin, in IEEE Topical Meet. on Silicon Monolit. Integr. Circ. in RF Syst., SiRF '08, (Orlando, FL), pp. 151–154, 23-25 Jan 2008.

[10] D. Lederer and J.-P. Raskin, "New substrate passivation method dedicated to HR SOI wafer fabrication with increased substrate resistivity" IEEE Electron Device Letters, vol. 26, no. 11, pp. 805-807, Nov. 2005.