Post-Process Local Porous Silicon Integration Method for RF Application

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Synopsis

Why ?

How ?

What ?

Porous silicon for

Strategic choice for RF applications

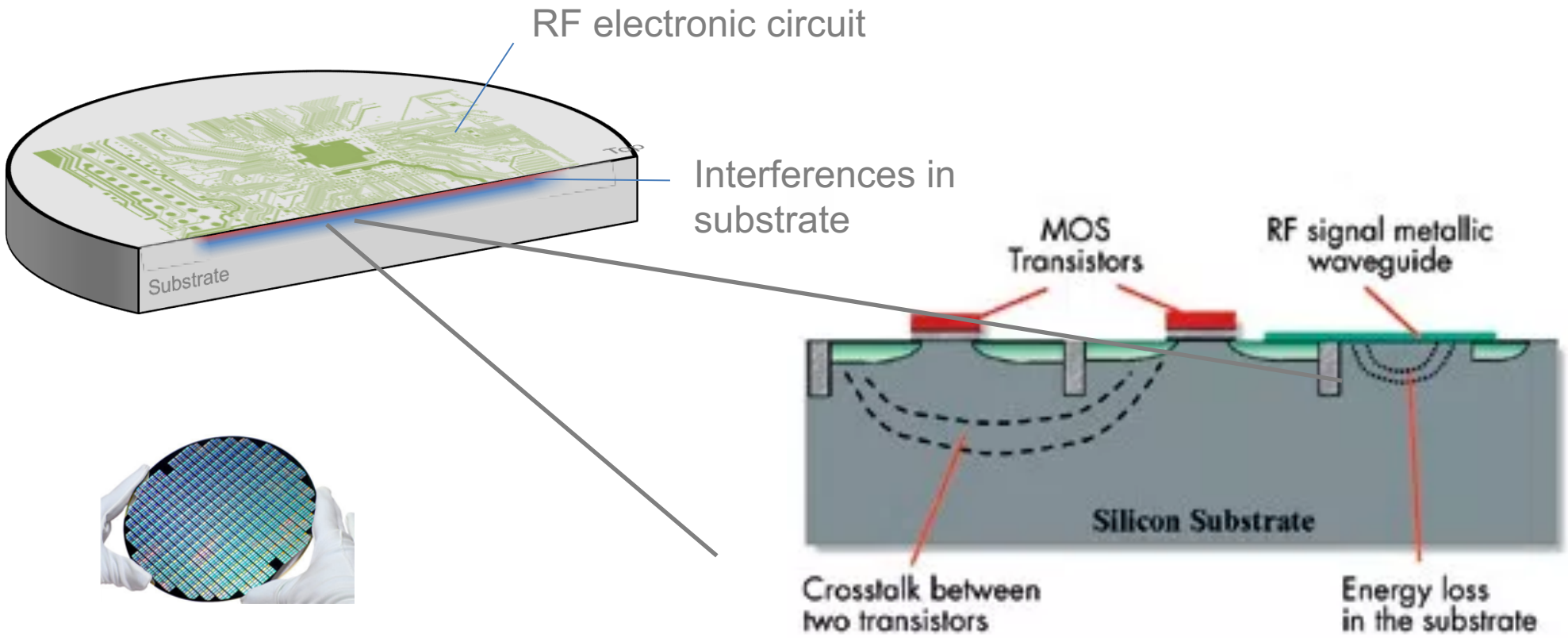
Co-integration
Digital/Analog and RF FEM

Silicon
still interesting?

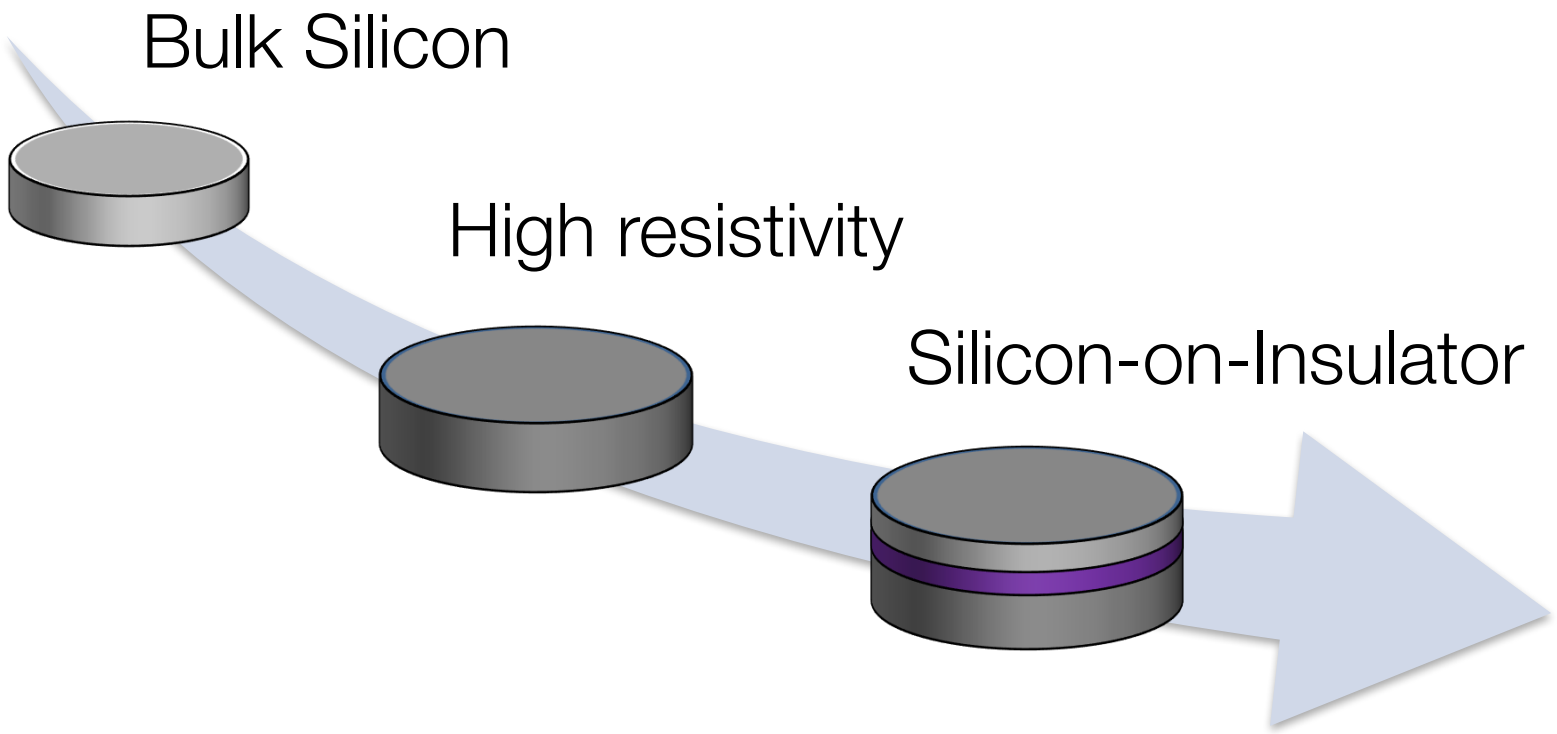
Excellent control
of Si process

Low production cost
of the substrate

Silicon Substrate



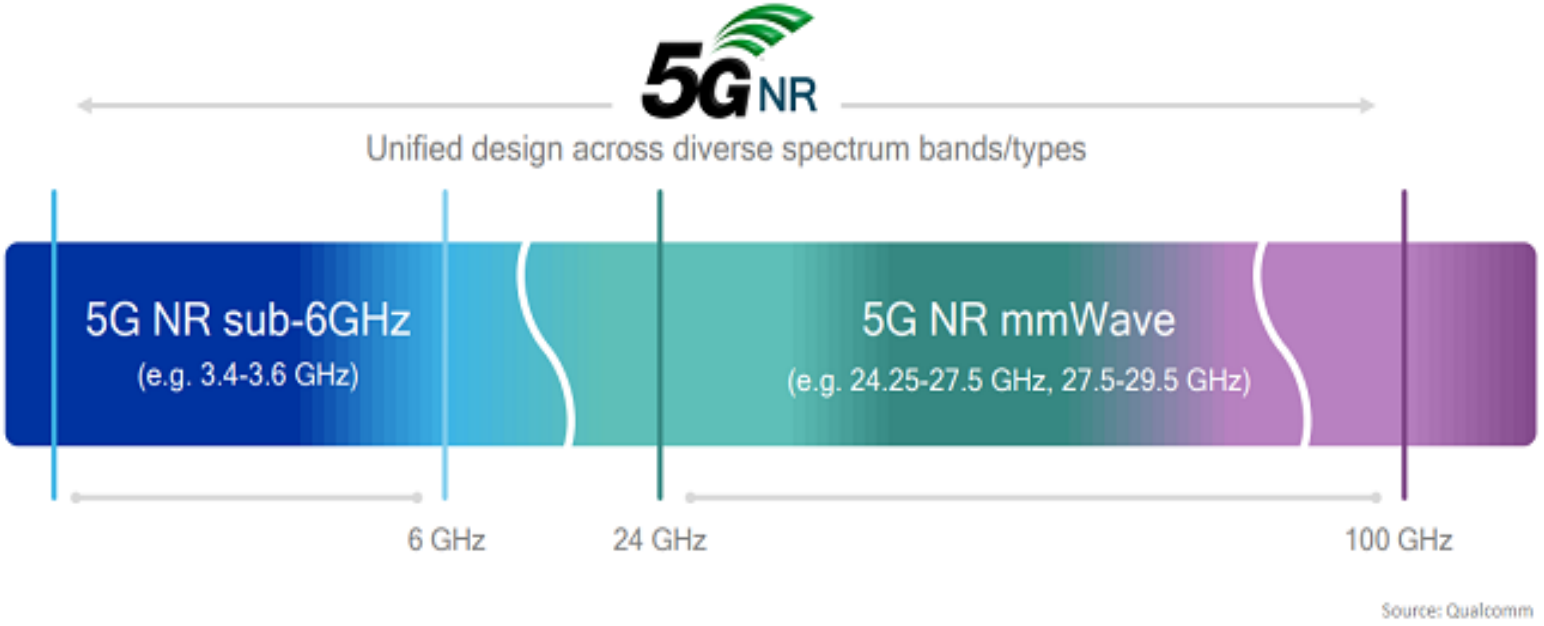
Only mechanical support?



Trap-rich HR-SOI

Benchmark

RF silicon substrate history



High Linearity Level

High Isolation Level

Silicon, the Substrate for 5G?

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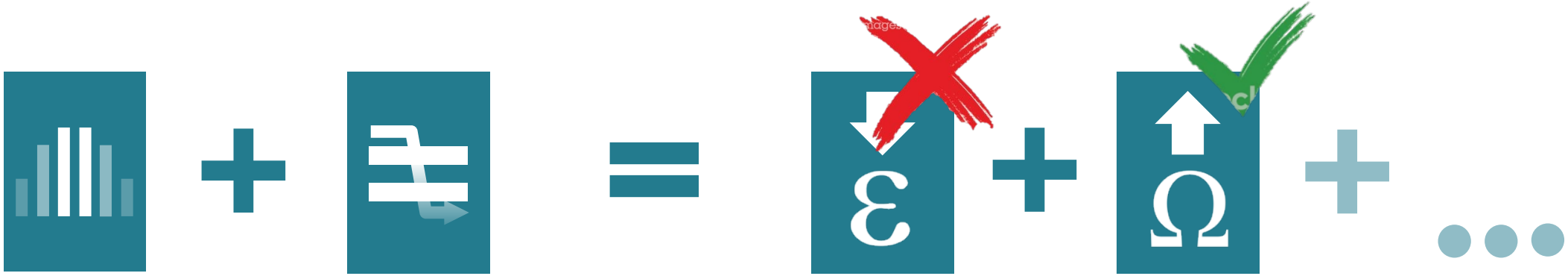
Trap-rich HR-SOI

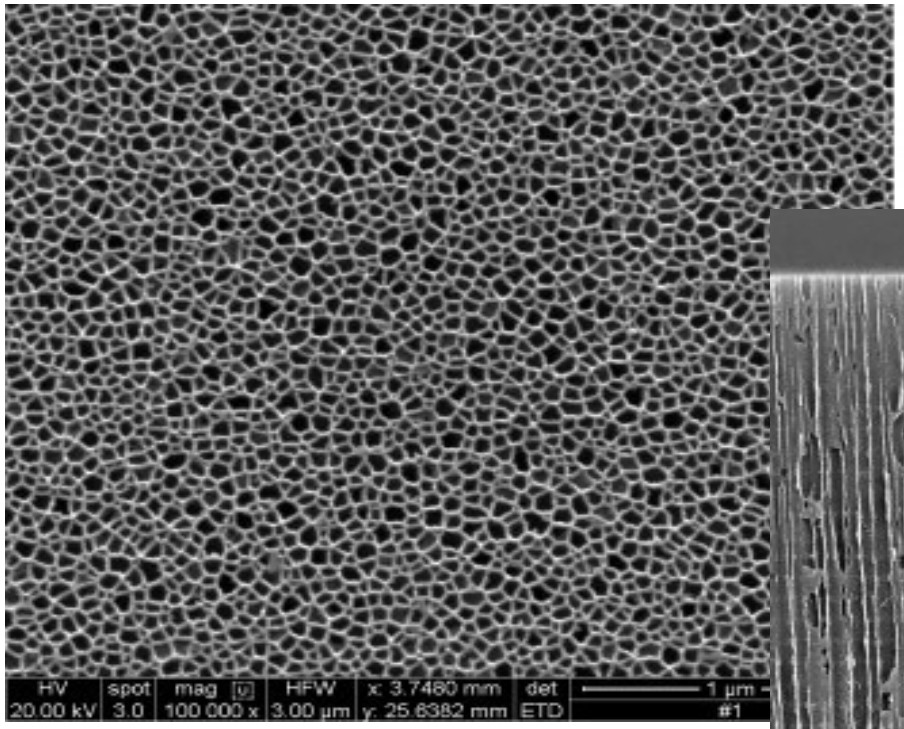


Silicon, the Substrate for 5G?

How can we reduce

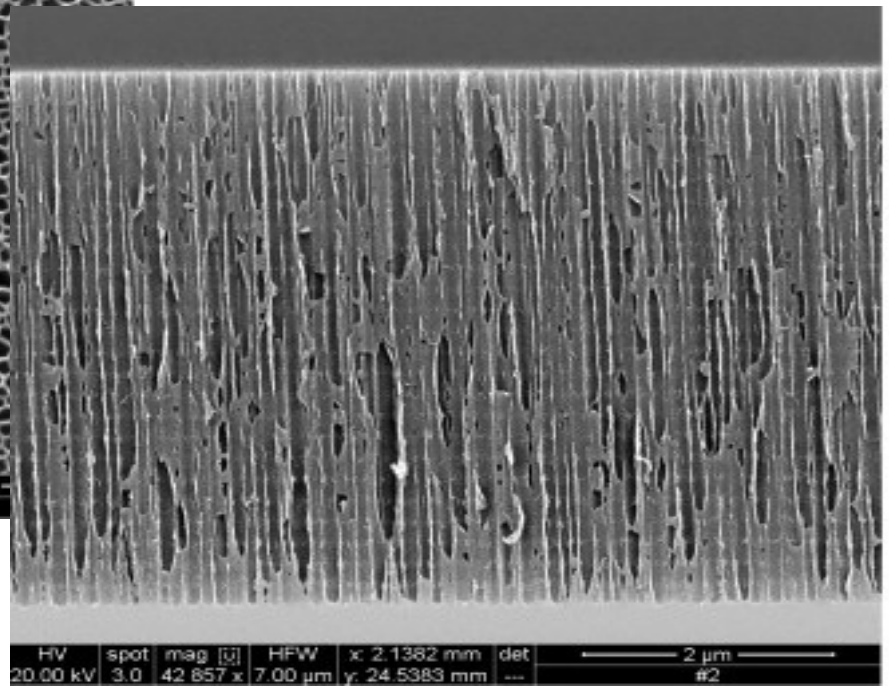
the permittivity of silicon?

The question …

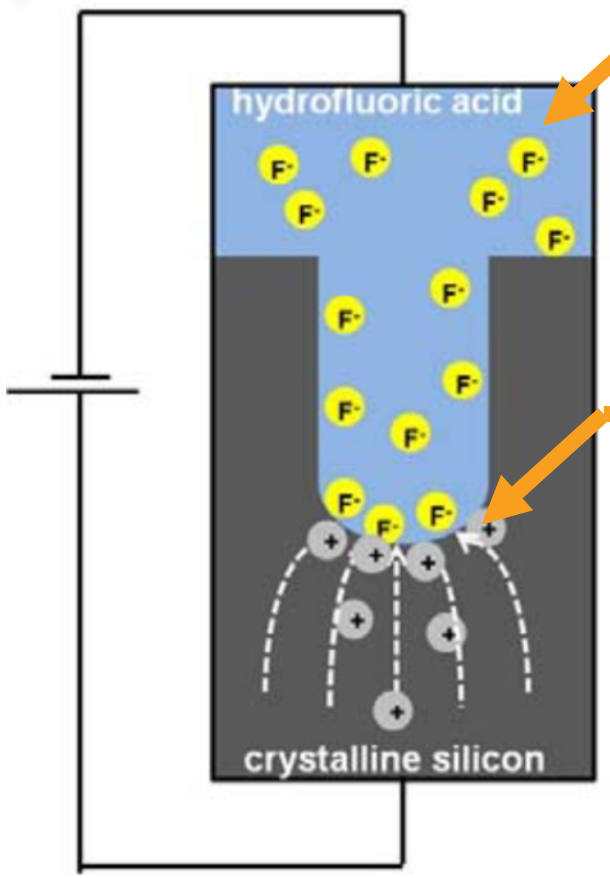


< Top view

Cross-section view >



Porous Silicon, the solution?



F ions in electrolyte

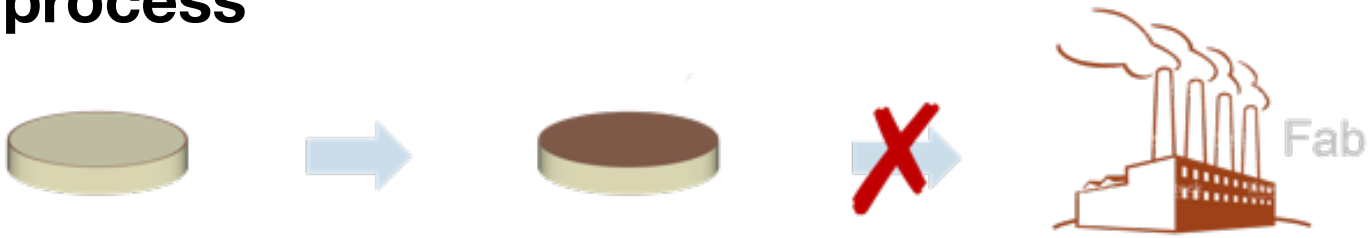
Holes in Silicon

$$Si + 6\,F^- + 2\,H^+ + 2\,h^+ \rightarrow SiF_6^{2-} + H_2$$

Holes attracted by peak effect.

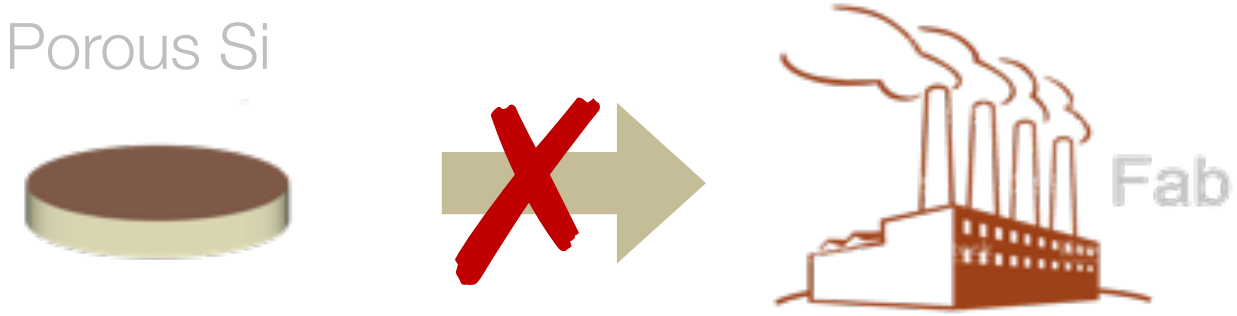
Etching at the tip.

PRE-process



Porous silicon is produced
before the foundry steps

Usual approach



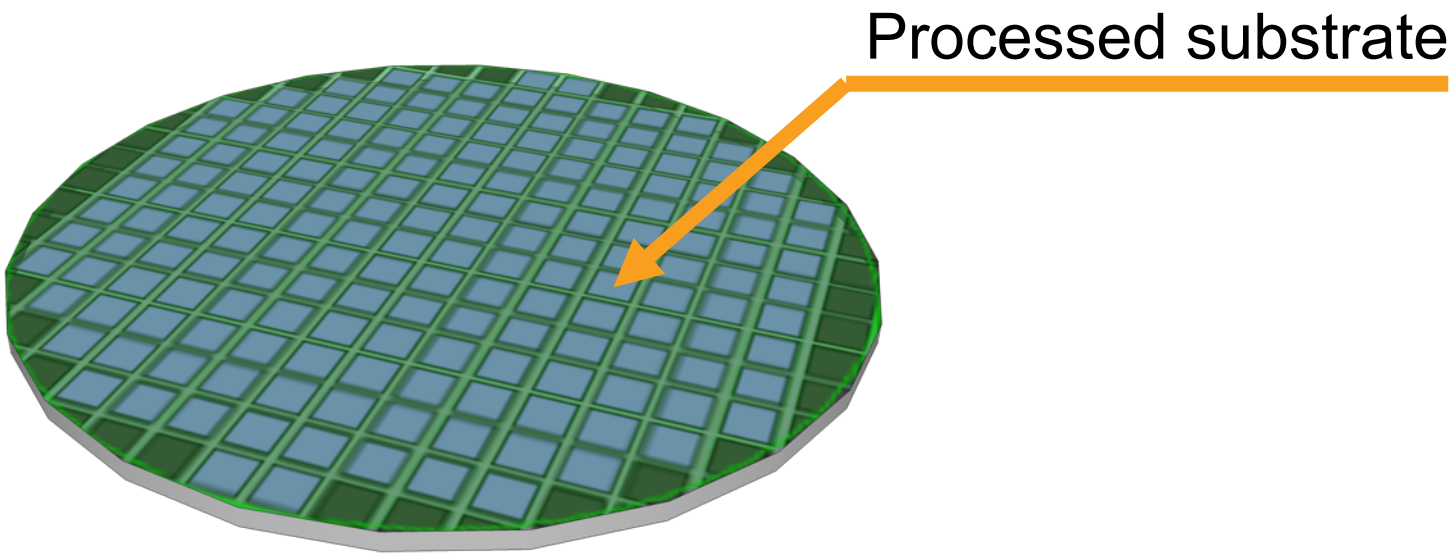
Strongly CMOS-Incompatible

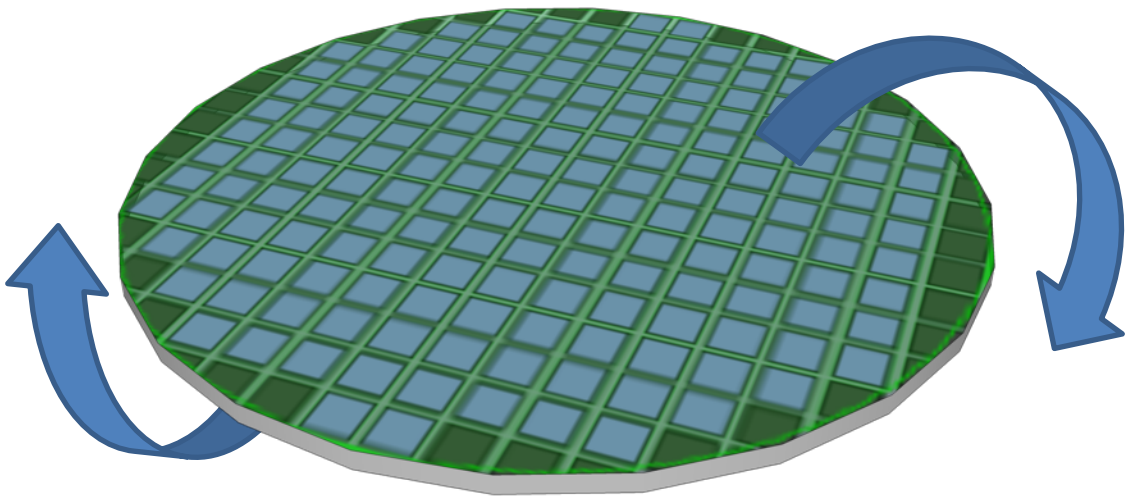
- Wafer bending
- Large roughness
- Annealing limitations
- Strong Impact

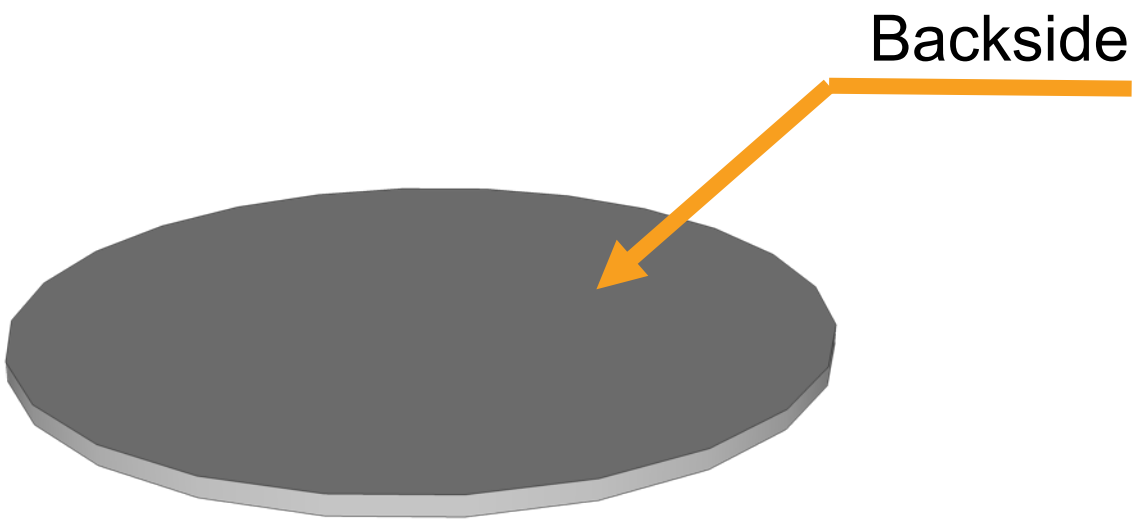
PRE-process

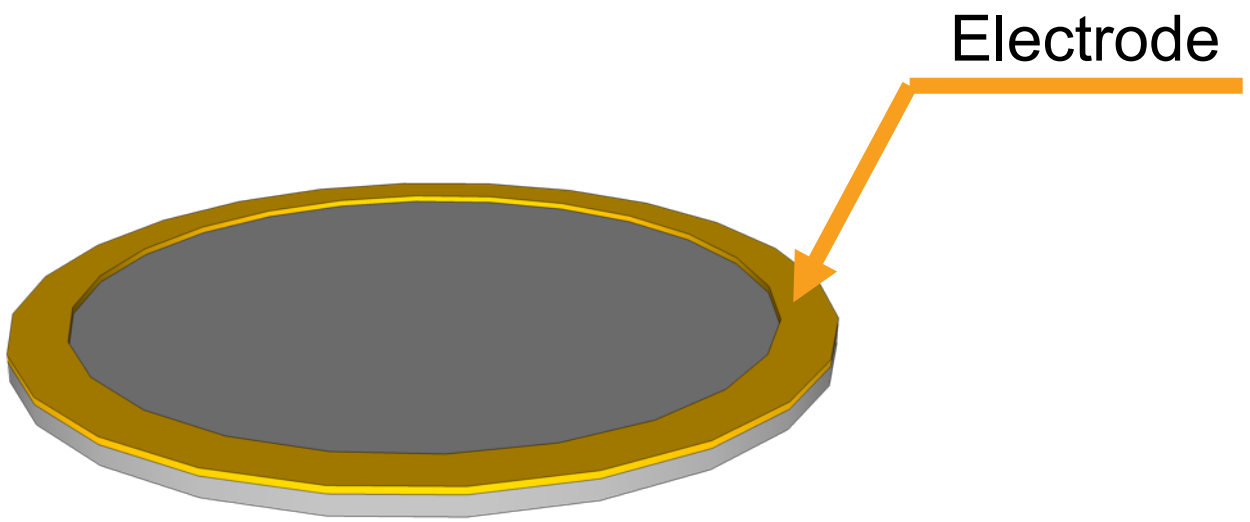
POST-process

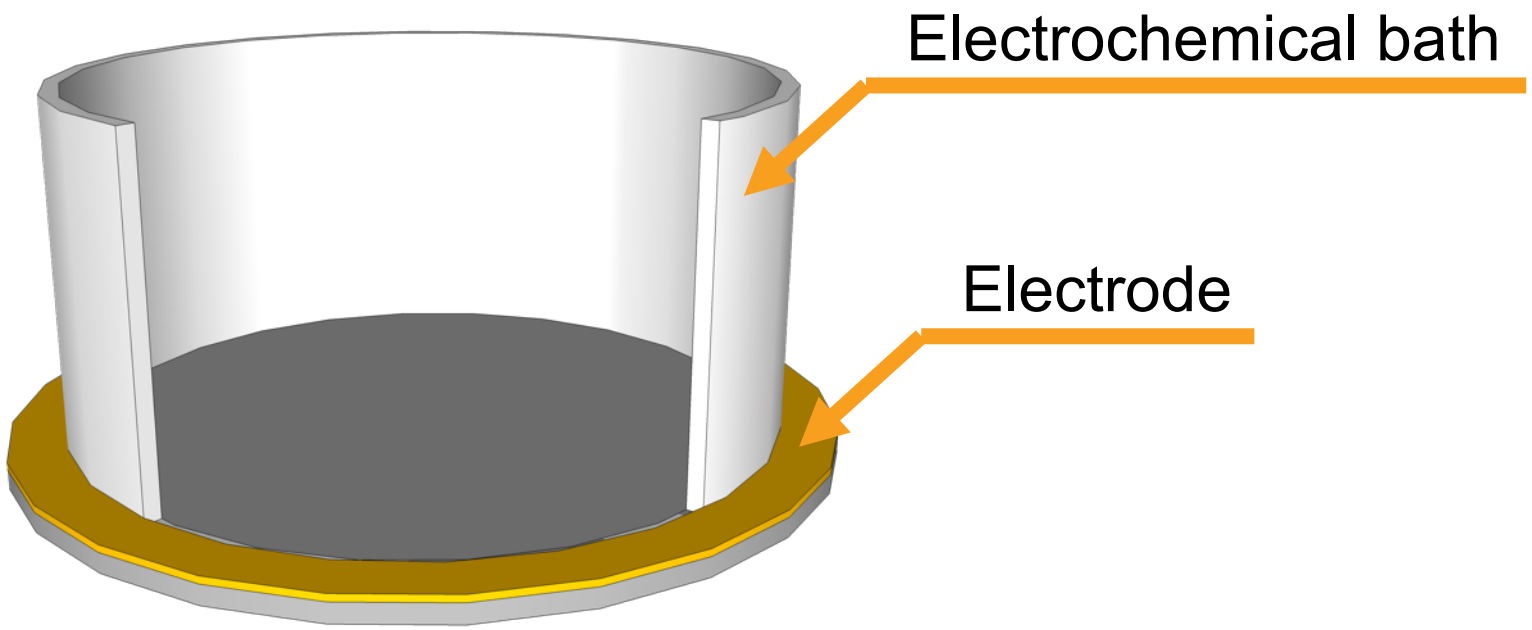
Innovative approach

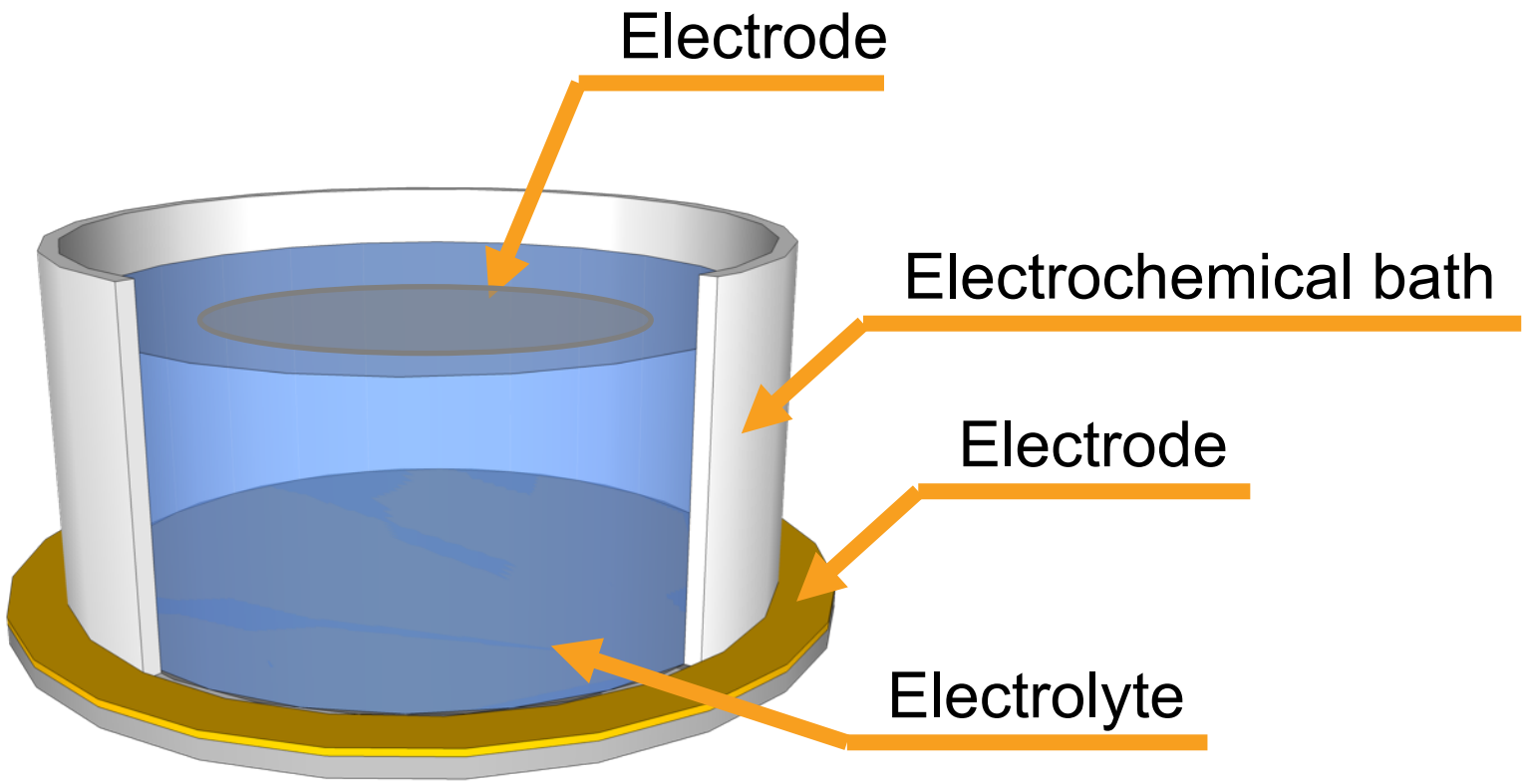

Processed substrate

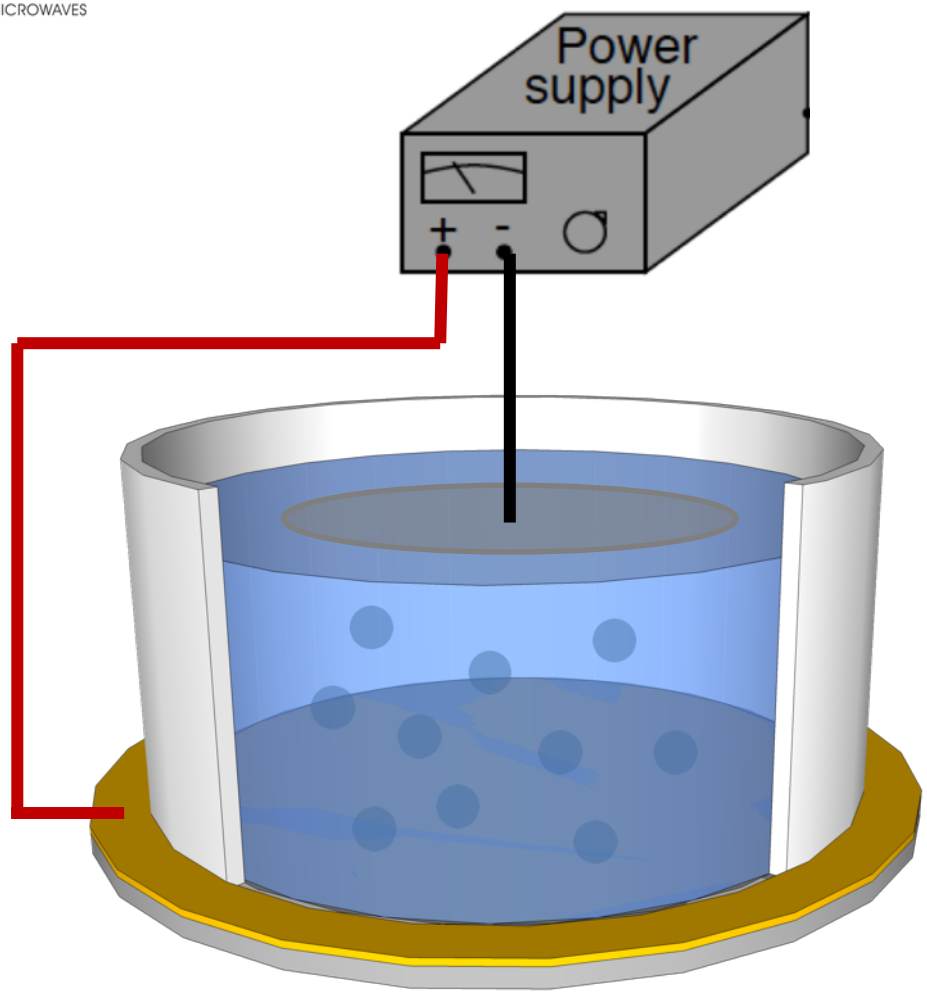


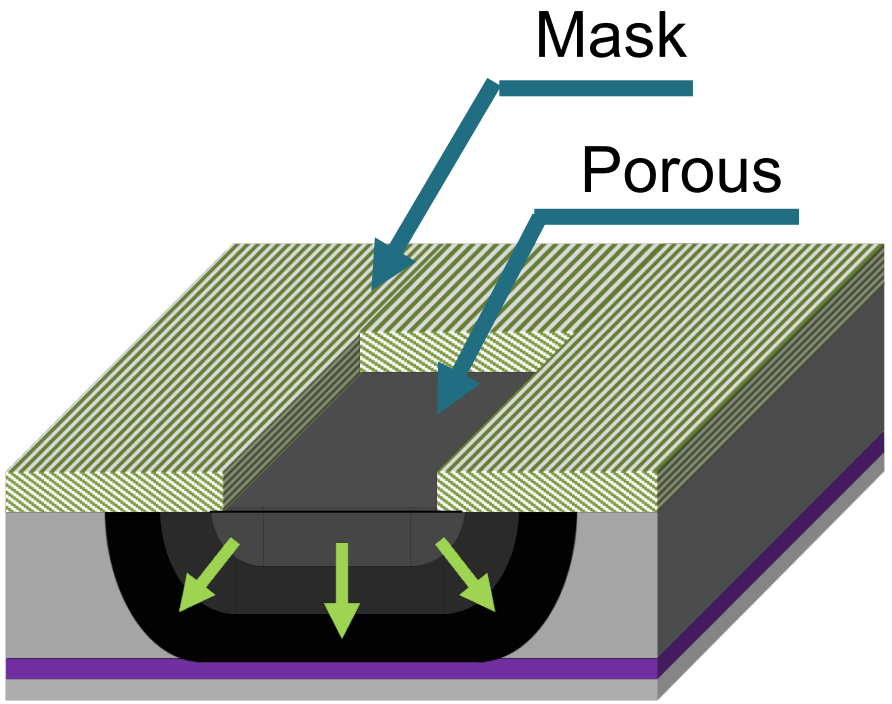

Backside

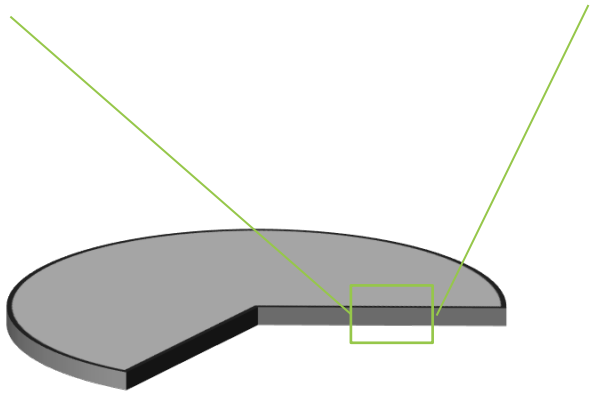

Electrode

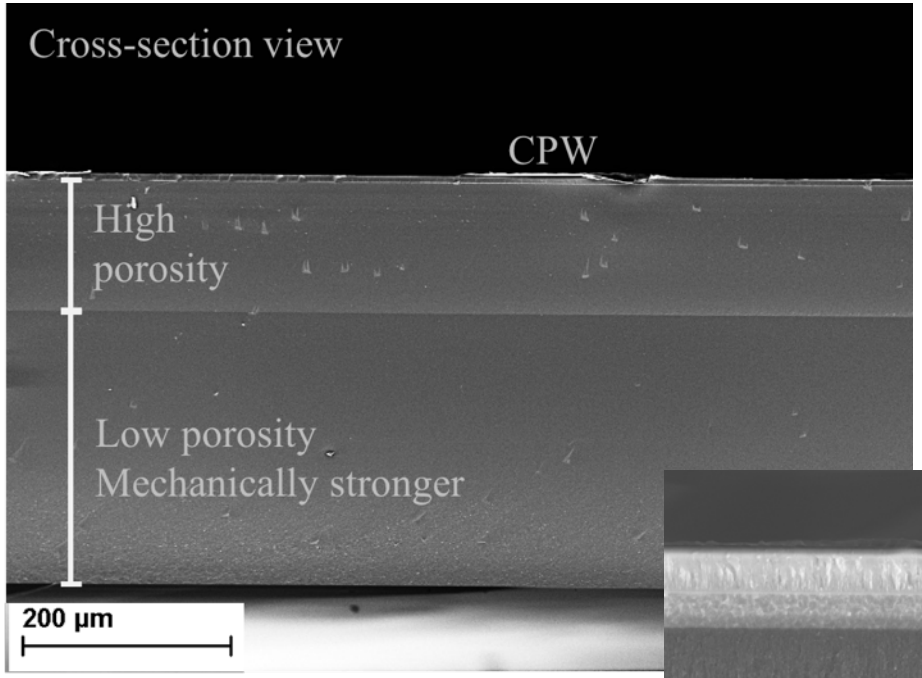

Electrochemical bath
Electrode

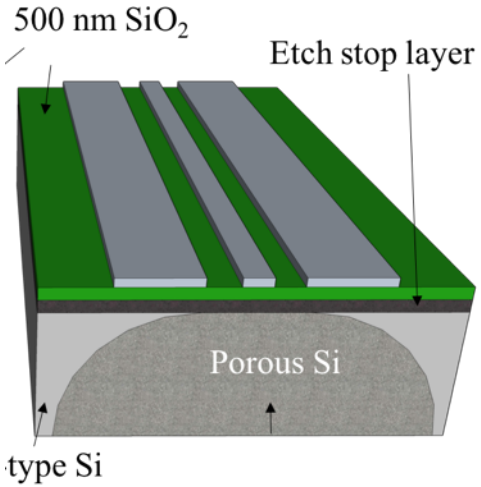

Electrode
Electrochemical bath
Electrode
Electrolyte

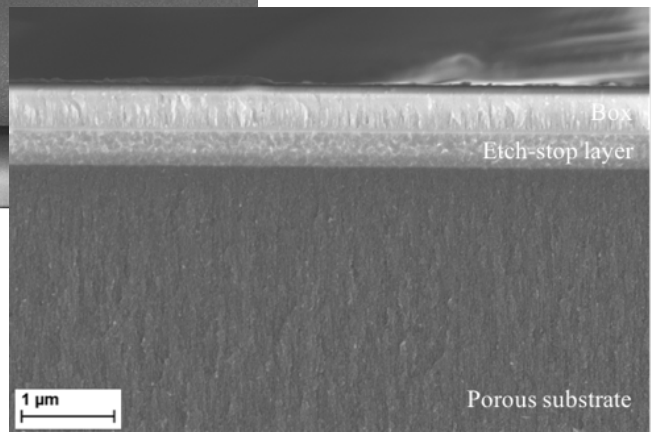

Power
supply
+
-

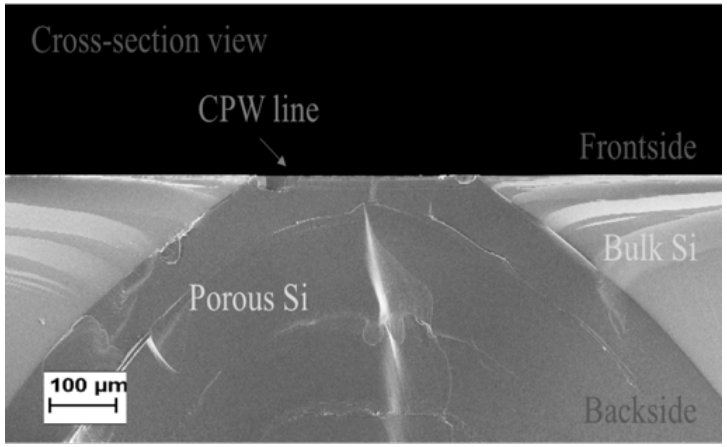

Mask
Porous



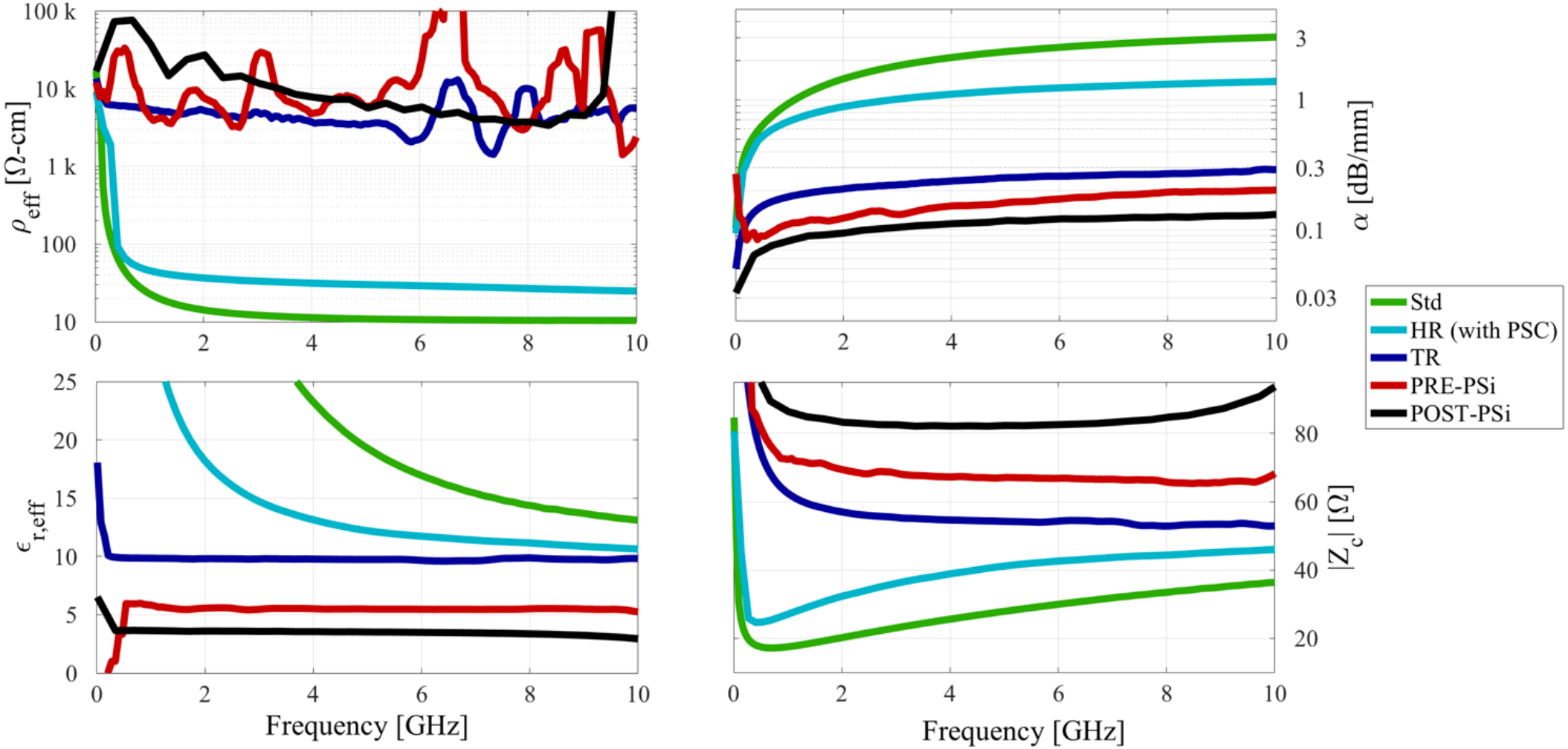


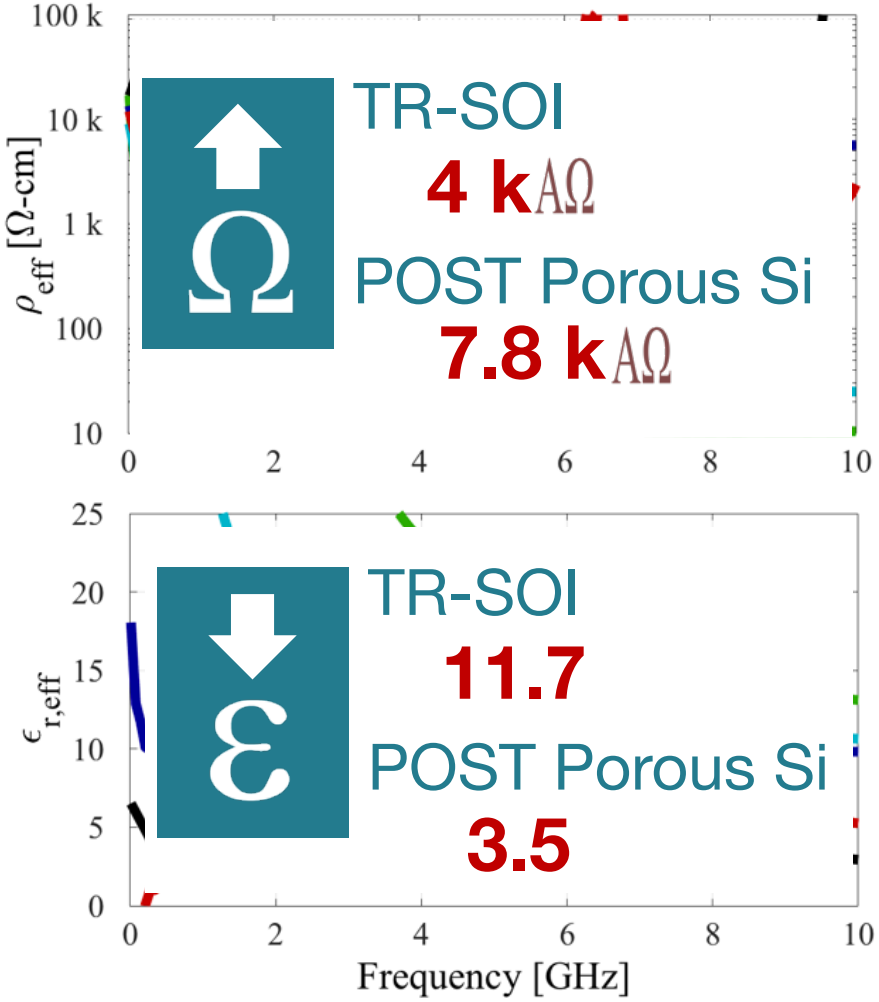


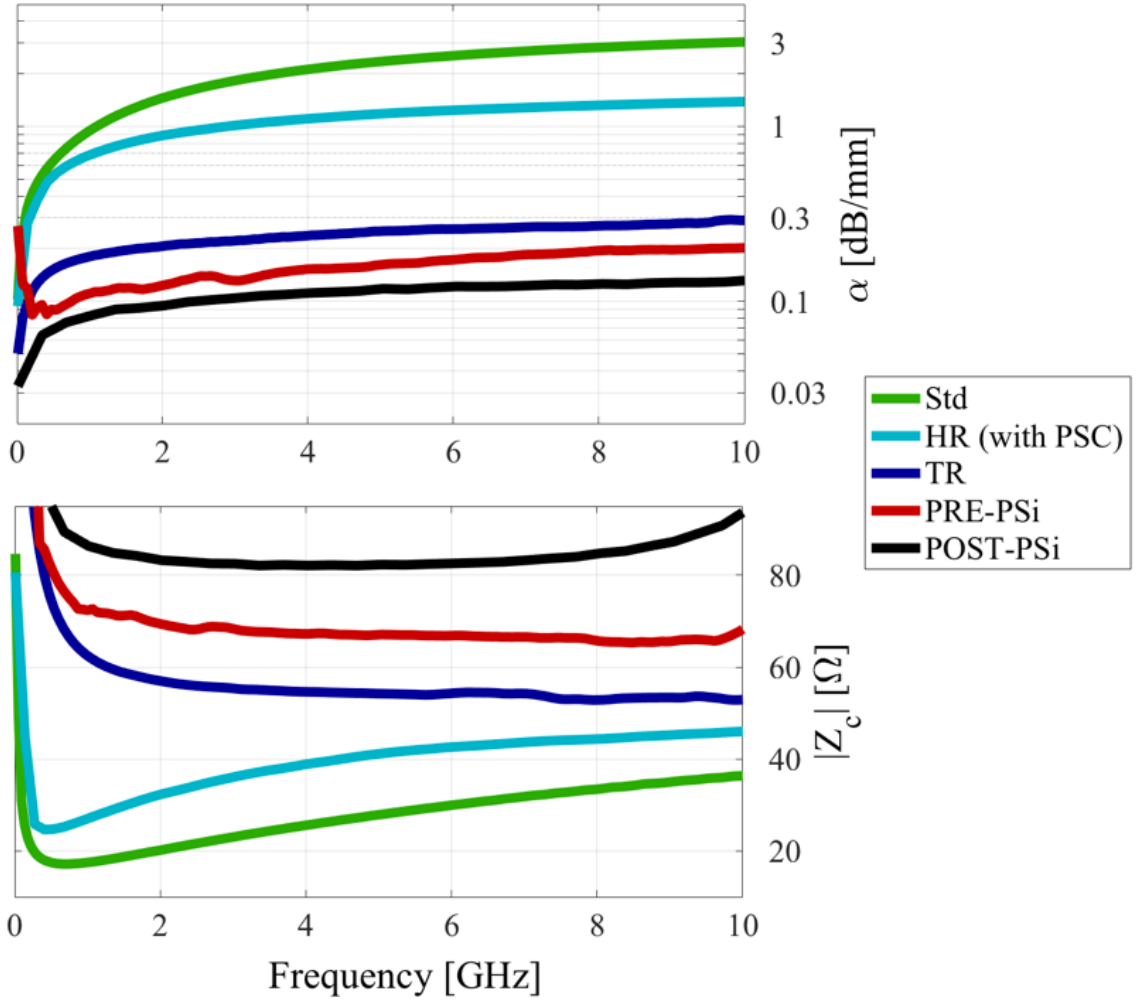


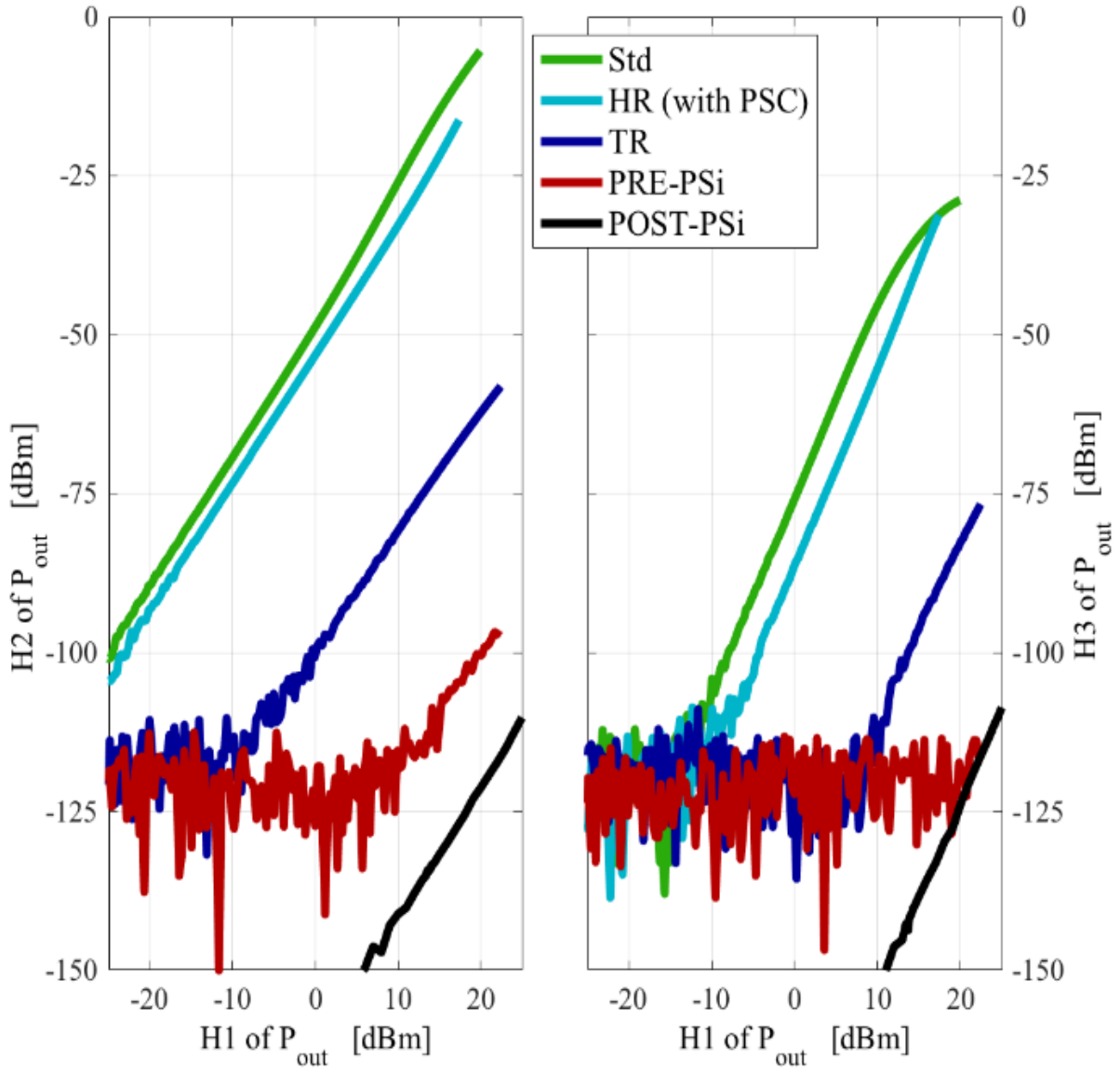


Post-process porous silicon Technology


100 k
10 k
1 k
100
10
ρ_{eff} [Ω-cm]
0
2
4
6
8
10
3
1
0.3
0.1
0.03
α [dB/mm]
Std
HR (with PSC)
TR
PRE-PSi
POST-PSi
25
20
15
10
5
0
$\epsilon_{r,eff}$
Frequency [GHz]
80
60
40
20
$|Z_c|$ [Ω]
Frequency [GHz]


TR-SOI
4 kΩ
POST Porous Si
7.8 kΩ
TR-SOI
11.7
POST Porous Si
3.5
ρ_{eff} [Ω-cm]
$\epsilon_{r,eff}$
Frequency [GHz]


α [dB/mm]
|Z_c| [Ω]
Frequency [GHz]
Std
HR (with PSC)
TR
PRE-PSi
POST-PSi



Linearity

TR-SOI

-75 dBm

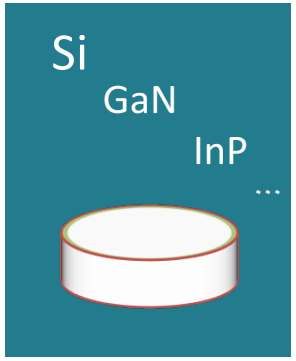
POST Porous Si

-130 dBm

Conclusions

High Performances

CMOS-compatible



Something-on-porous silicon

Great flexibility